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Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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HD74LS112

Dual J-K Negative-edge-triggered Flip-Flops (with Preset and Clear)

REJ03D0426-0300

Rev.3.00

Jul.13.2005

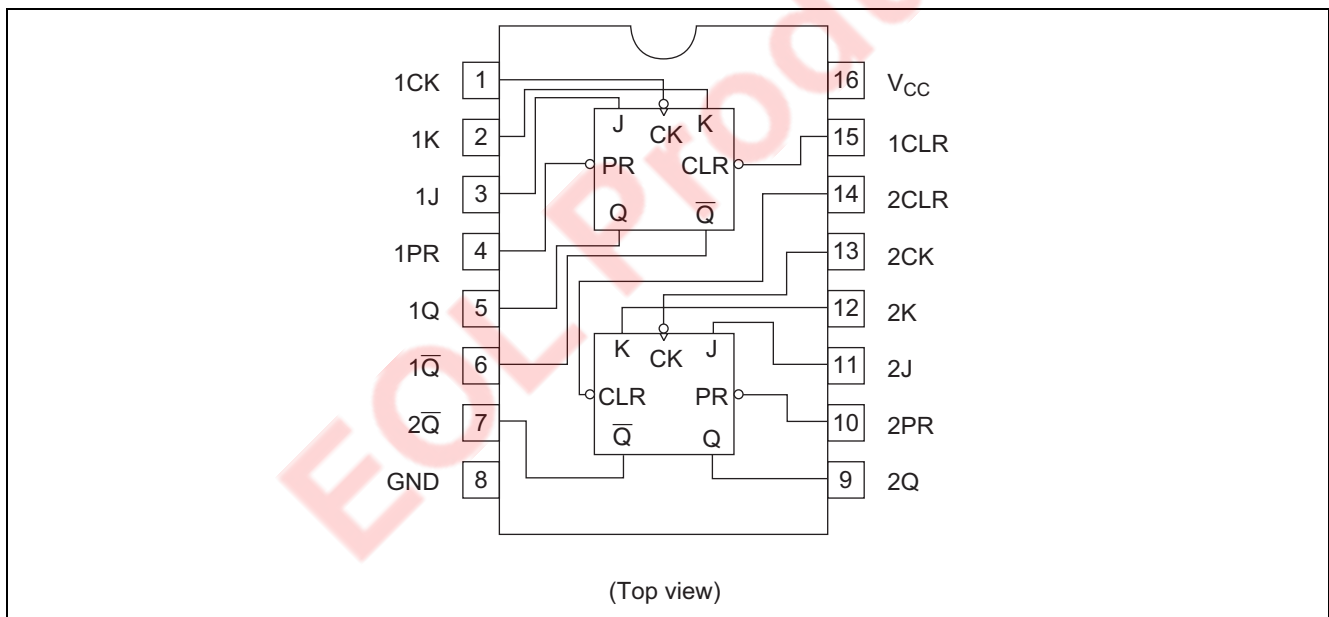
Features

- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LS112P	DILP-16 pin	PRDP0016AE-B (DP-16FV)	P	—
HD74LS112FPEL	SOP-16 pin (JEITA)	PRSP0016DH-B (FP-16DAV)	FP	EL (2,000 pcs/reel)
HD74LS112RPEL	SOP-16 pin (JEDEC)	PRSP0016DG-A (FP-16DNV)	RP	EL (2,500 pcs/reel)

Note: Please consult the sales office for the above package availability.

Pin Arrangement



Function Table

Inputs					Outputs	
Preset	Clear	Clock	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_o	$\bar{Q}_o$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Toggle	
H	H	H	X	X	Q_o	$\bar{Q}_o$

Notes: H; high level, L; low level, X; irrelevant

↓; transition from high to low level

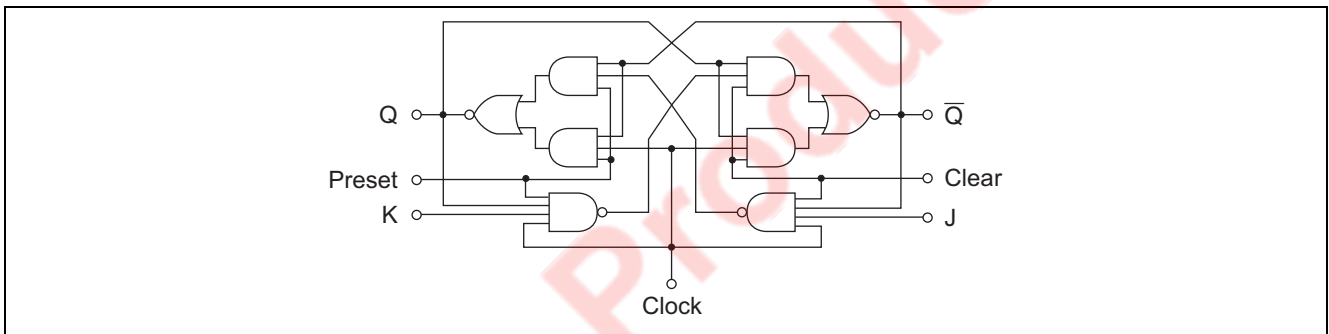
Q_o ; level of Q before the indicated steady-state input conditions were established.

$\bar{Q}_o$; complement of Q_o or level of $\bar{Q}$ before the indicated steady-state input conditions were established.

Toggle; each output changes to the complement of its previous level on each active transition indicated by ↓.

*; This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

Block Diagram (1/2)



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	V_{CC}	7	V
Input voltage	V_{IN}	7	V
Power dissipation	P_T	400	mW
Storage temperature	Tstg	-65 to +150	°C

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

Recommended Operating Conditions

Item		Symbol	Min	Typ	Max	Unit
Supply voltage		V_{CC}	4.75	5.00	5.25	V
Output current		I_{OH}	—	—	−400	μA
		I_{OL}	—	—	8	mA
Operating temperature		T_{opr}	−20	25	75	°C
Clock frequency		f_{clock}	0	—	30	MHz
Pulse width	Clock High	t_w	20	—	—	ns
	Clear Preset Low		25	—	—	ns
Setup time	“H” Data	t_{su}	20↓	—	—	ns
	“L” Data		20↓	—	—	ns
Hold time		t_h	0↓	—	—	ns

Electrical Characteristics

(Ta = −20 to +75 °C)

Item		Symbol	min.	typ.*	max.	Unit	Condition
Input voltage		V_{IH}	2.0	—	—	V	
		V_{IL}	—	—	0.8	V	
Output voltage		V_{OH}	2.7	—	—	V	$V_{CC} = 4.75 \text{ V}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OH} = -400 \mu A$
		V_{OL}	—	—	0.5	V	$I_{OL} = 8 \text{ mA}$
			—	—	0.4	V	$V_{CC} = 4.75 \text{ V}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OL} = 4 \text{ mA}$
Input current	J, K	I_{IH}	—	—	20	μA	$V_{CC} = 5.25 \text{ V}$, $V_I = 2.7 \text{ V}$
	Clear		—	—	60	μA	
	Preset		—	—	60	μA	
	Clock		—	—	80	μA	
	J, K	I_{IL}^{**}	—	—	−0.4	mA	$V_{CC} = 5.25 \text{ V}$, $V_I = 0.4 \text{ V}$
	Clear		—	—	−0.8	mA	
	Preset		—	—	−0.8	mA	
	Clock		—	—	−0.8	mA	
	J, K	I_I	—	—	0.1	mA	$V_{CC} = 5.25 \text{ V}$, $V_I = 7 \text{ V}$
	Clear		—	—	0.3	mA	
	Preset		—	—	0.3	mA	
	Clock		—	—	0.4	mA	
Short-circuit output current		I_{OS}	−20	—	−100	mA	$V_{CC} = 5.25 \text{ V}$
Supply current***		I_{CC}	—	4	8	mA	$V_{CC} = 5.25 \text{ V}$
Input clamp voltage		V_{IK}	—	—	−1.5	V	$V_{CC} = 4.75 \text{ V}$, $I_{IN} = -18 \text{ mA}$

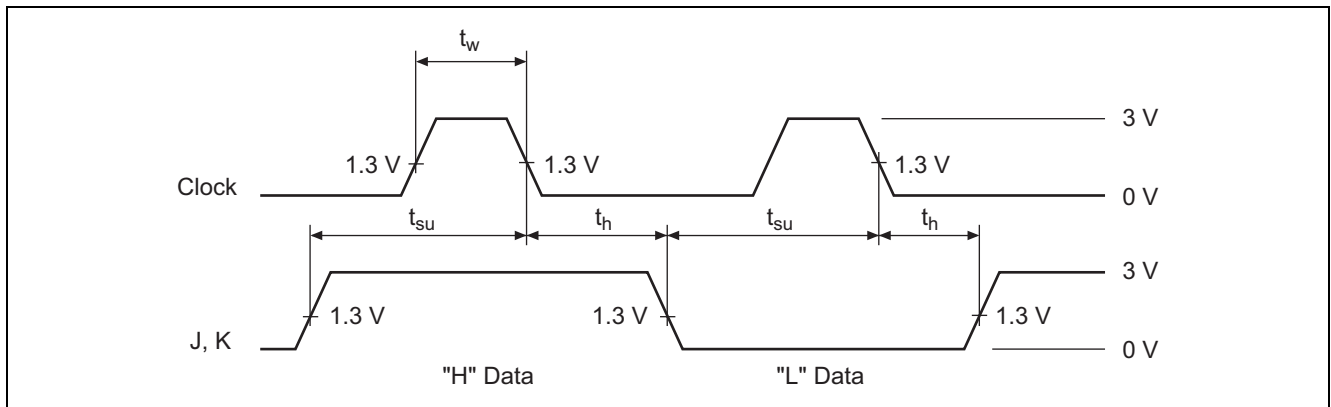
Notes: * $V_{CC} = 5 \text{ V}$, $T_a = 25^\circ\text{C}$ ** I_{IL} should not be measured when preset and clear inputs are low at same time.*** With all outputs open, I_{CC} is measured with the Q and $\bar{Q}$ outputs high in turn. At the times of measurement, the clock input is grounded.

Switching Characteristics

(V_{CC} = 5 V, T_a = 25°C)

Item	Symbol	Inputs	Outputs	min.	typ.	max.	Unit	Condition
Maximum clock frequency	f_{max}			30	45	—	MHz	$C_L = 15 \text{ pF}$, $R_L = 2 \text{ k}\Omega$
Propagation delay time	t_{PLH}	Clear Preset Clock	Q, $\bar{Q}$	—	11	20	ns	
	t_{PHL}			—	15	30	ns	

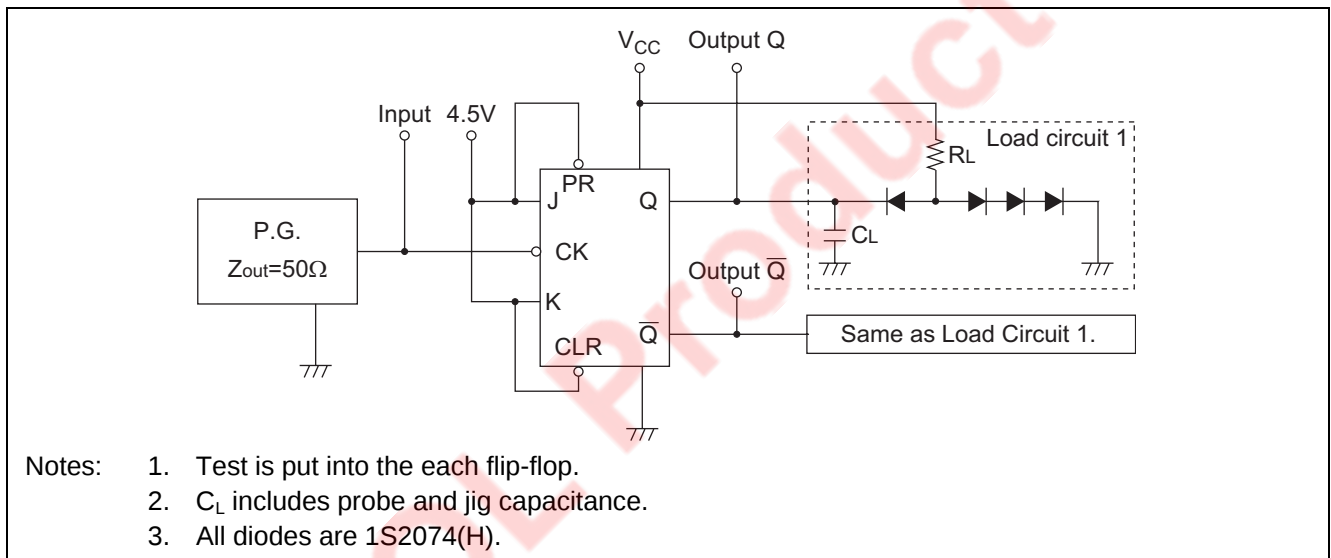
Timing Definition



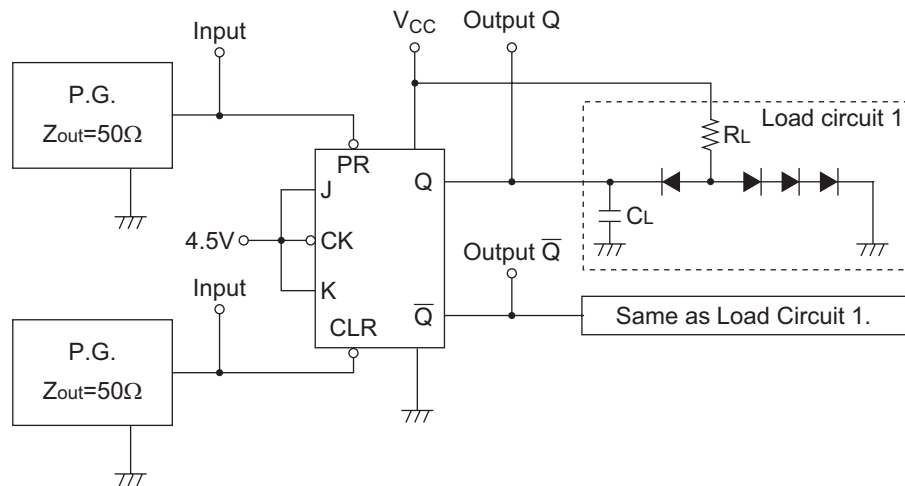
Testing Method

Test Circuit

1. f_{max} , t_{PLH} , t_{PHL} , (Clock $\rightarrow$ Q, $\bar{Q}$)

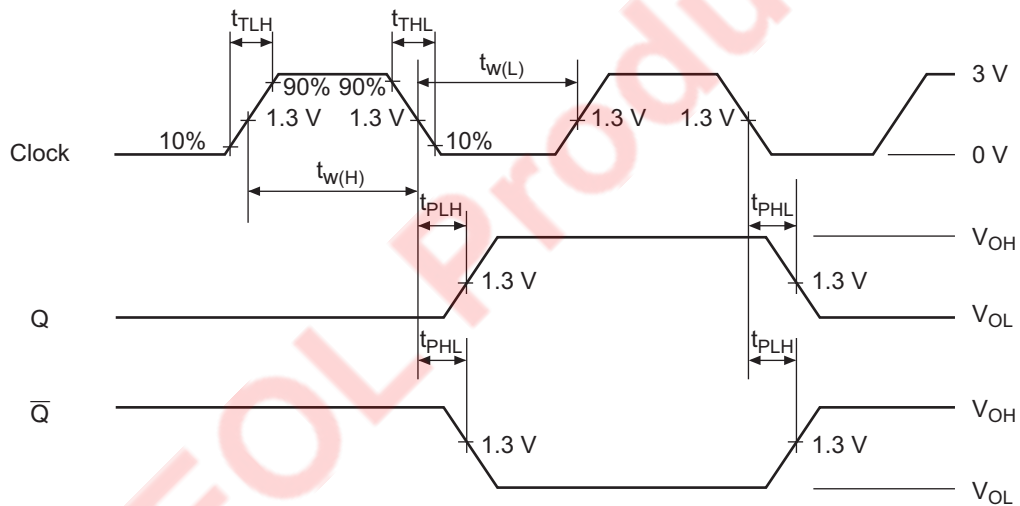


2. t_{PHL} , t_{PLH} , (Clear, Preset $\rightarrow$ Q, $\bar{Q}$)



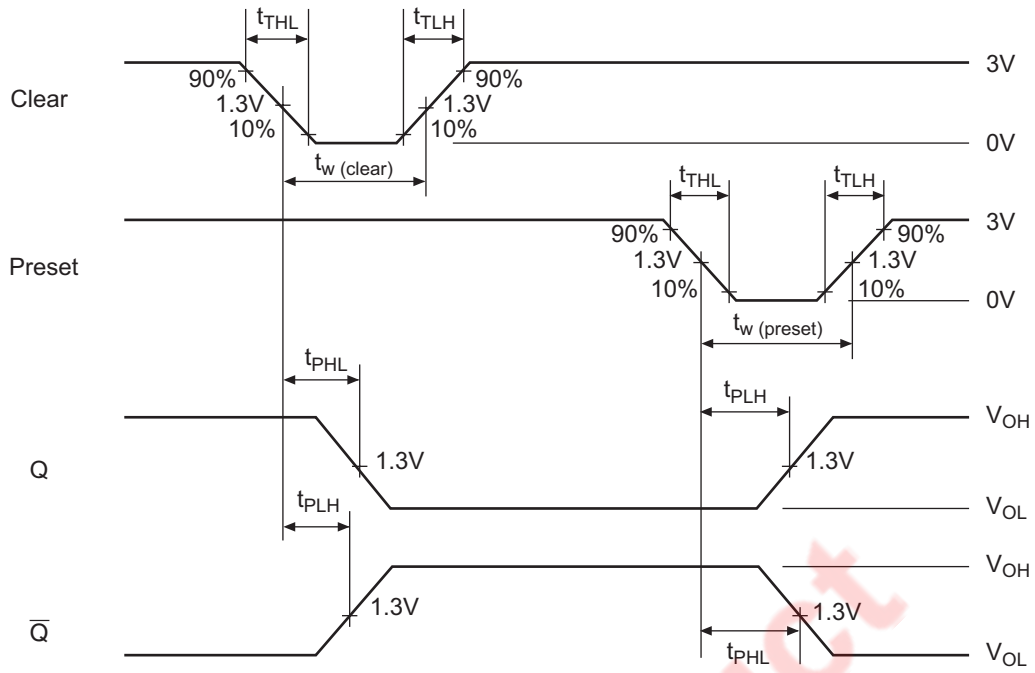
- Notes:
1. Test is put into the each flip-flop.
 2. C_L includes probe and jig capacitance.
 3. All diodes are 1S2074(H).

Waveforms 1



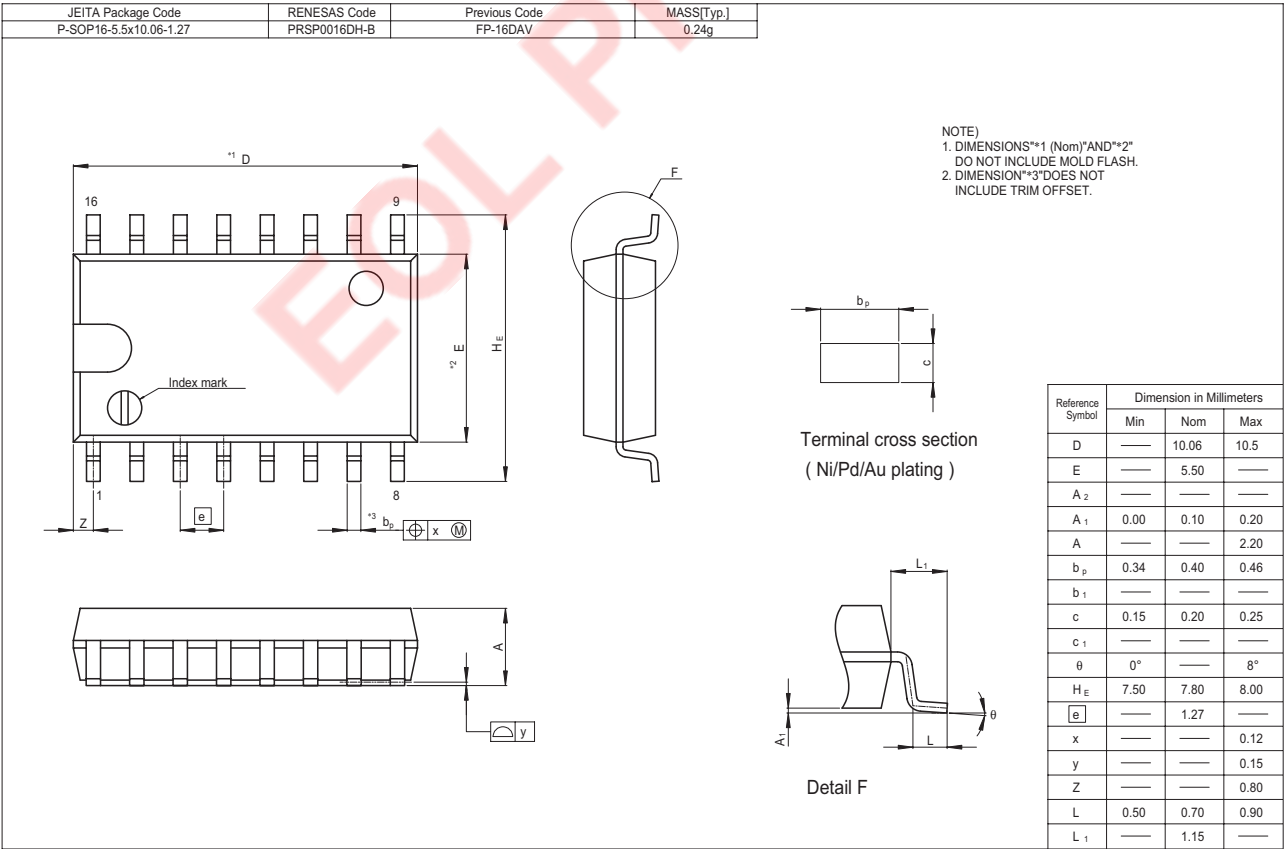
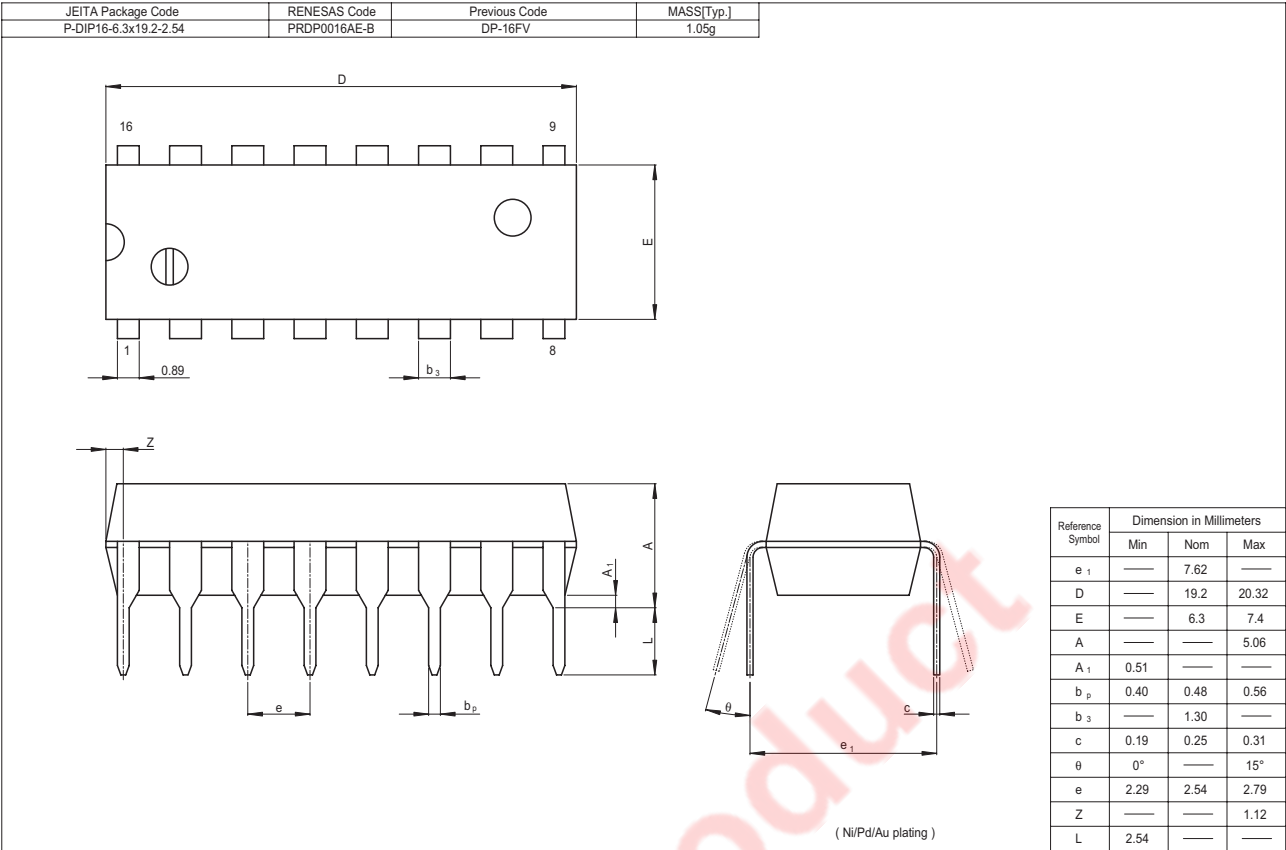
Note: Clock input pulse: $t_{TLH} \leq 15$ ns, $t_{THL} \leq 6$ ns, PRR = 1 MHz, duty cycle = 50%
and: for f_{max} , t_{THL} $t_{THL} \leq 2.5$ ns.

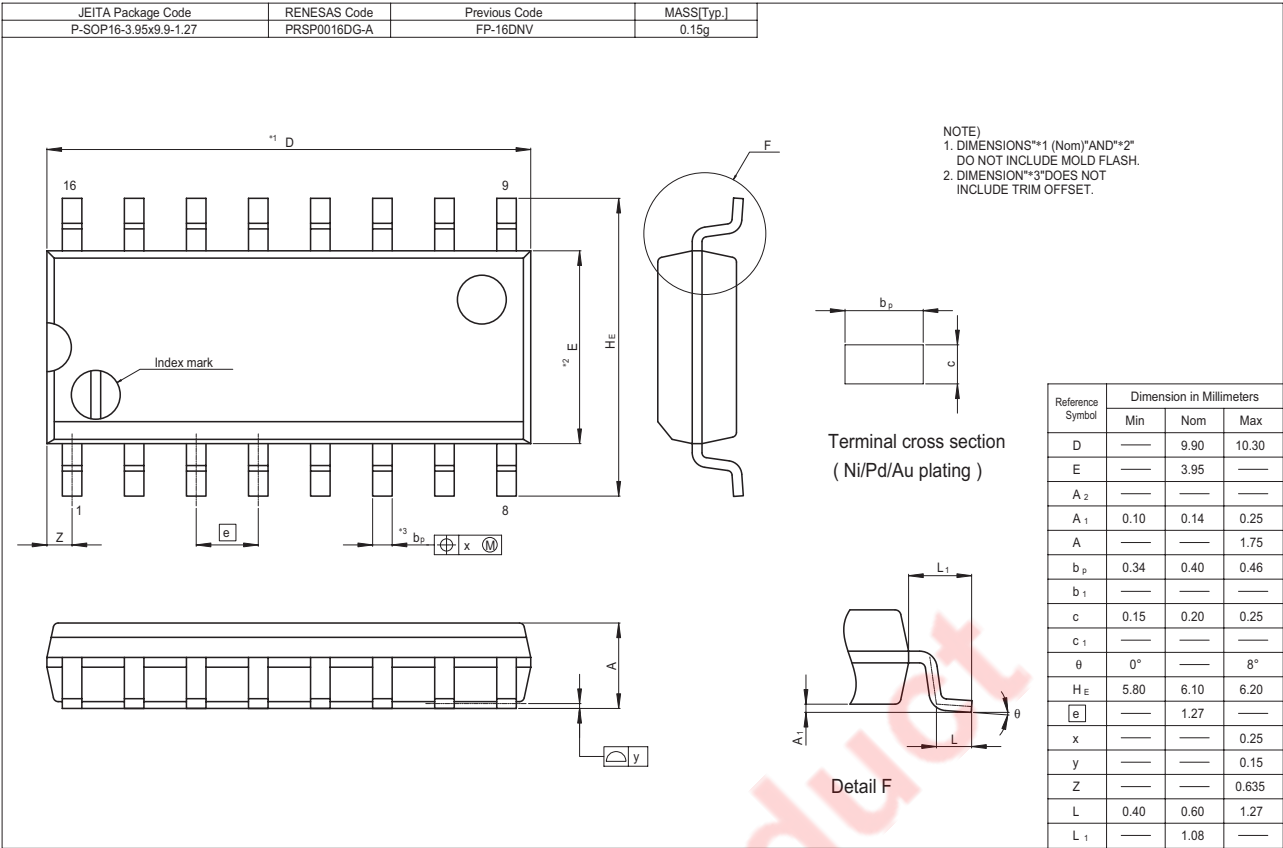
Waveforms 2



Note: Clear and clock input pulse: $t_{TLH} \leq 15$ ns, $t_{THL} \leq 6$ ns, PRR = 1 MHz.

Package Dimensions





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