

# HEF4051B

## 8-channel analog multiplexer/demultiplexer

Rev. 04 — 12 January 2005

Product data sheet

### 1. General description

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The HEF4051B is an 8-channel analog multiplexer/demultiplexer with three address inputs (A0 to A2), an active LOW enable input ( $\bar{E}$ ), eight independent inputs/outputs (Y0 to Y7) and a common input/output (Z).

The device contains eight bidirectional analog switches, each with one side connected to an independent input/output (Y0 to Y7) and the other side connected to a common input/output (Z).

With  $\bar{E}$  LOW, one of the eight switches is selected (low-impedance ON-state) by A0 to A2. With  $\bar{E}$  HIGH, all switches are in the high-impedance OFF-state, independent of A0 to A2. If break before make is needed, then it is necessary to use the enable input.

$V_{DD}$  and  $V_{SS}$  are the supply voltage connections for the digital control inputs (A0 to A2, and  $\bar{E}$ ). The  $V_{DD}$  to  $V_{SS}$  range is 3 V to 15 V. The analog inputs/outputs (Y0 to Y7, and Z) can swing between  $V_{DD}$  as a positive limit and  $V_{EE}$  as a negative limit.  $V_{DD} - V_{EE}$  may not exceed 15 V.

For operation as a digital multiplexer/demultiplexer,  $V_{EE}$  is connected to  $V_{SS}$  (typically ground).

### 2. Features

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- Analog multiplexing and demultiplexing
- Digital multiplexing and demultiplexing
- Signal gating
- Multiple package option
- Specified from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$

**PHILIPS**

### 3. Quick reference data

**Table 1: Quick reference data**

$T_{amb} = 25\text{ }^{\circ}\text{C}$ ;  $R_L = 10\text{ k}\Omega$ ;  $C_L = 50\text{ pF}$ ;  $\bar{E} = V_{DD}$  (square wave);  $V_{is} = V_{DD} = 15\text{ V}$

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{PHZ}$	output disable time HIGH to OFF for $\bar{E}$ to Z or $\bar{E}$ to $Y_n$		-	85	170	ns
$t_{PLZ}$	output disable time LOW to OFF for $\bar{E}$ to Z or $\bar{E}$ to $Y_n$		-	115	230	ns
$t_{PZH}$ , $t_{PZL}$	output enable time OFF to HIGH or LOW for $\bar{E}$ to Z or $\bar{E}$ to $Y_n$		-	40	80	ns
$C_i$	input capacitance digital inputs		-	-	7.5	pF

### 4. Ordering information

**Table 2: Ordering information**

Type number	Package			
	Temperature range	Name	Description	Version
HEF4051BP	-40 °C to +85 °C	DIP16	plastic dual in-line package; 16 leads (300 mil); long body	SOT38-1
HEF4051BT	-40 °C to +85 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
HEF4051BTS	-40 °C to +85 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
HEF4051BTT	-40 °C to +85 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

5. Functional diagram

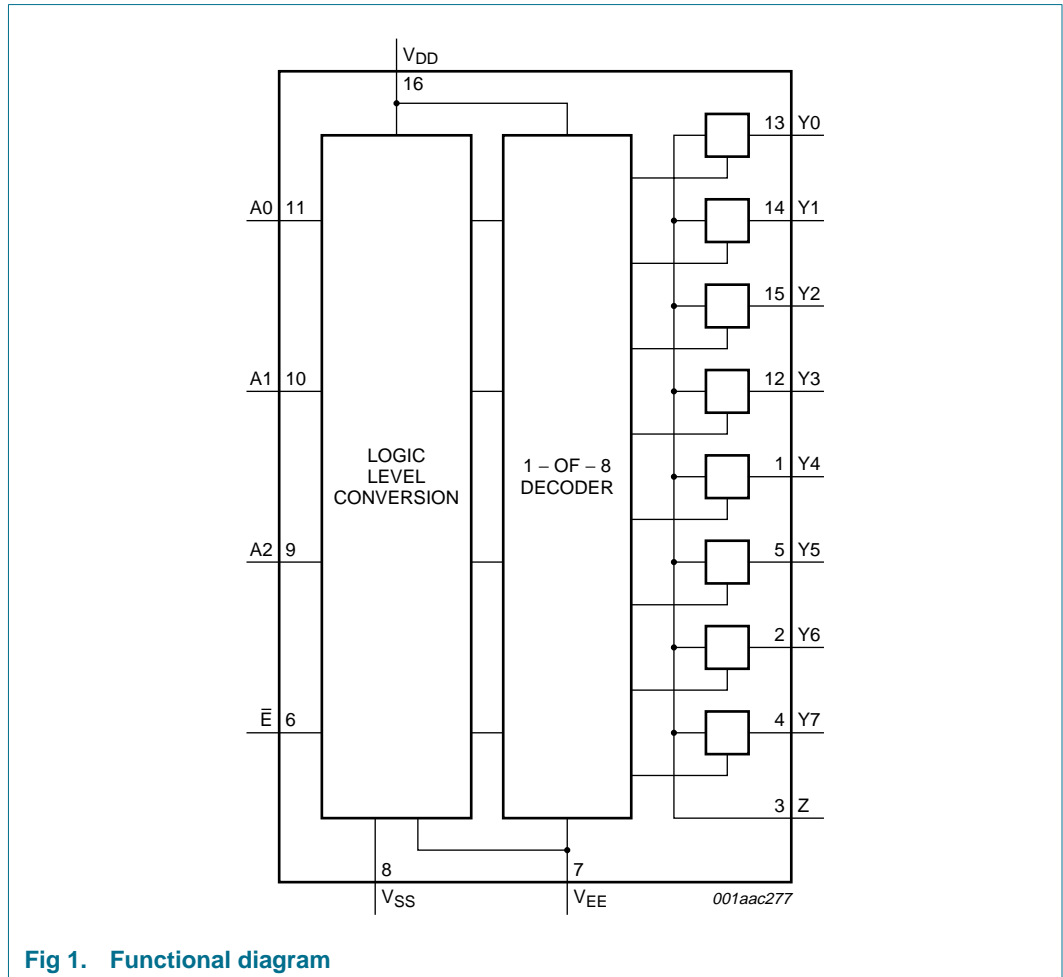


Fig 1. Functional diagram

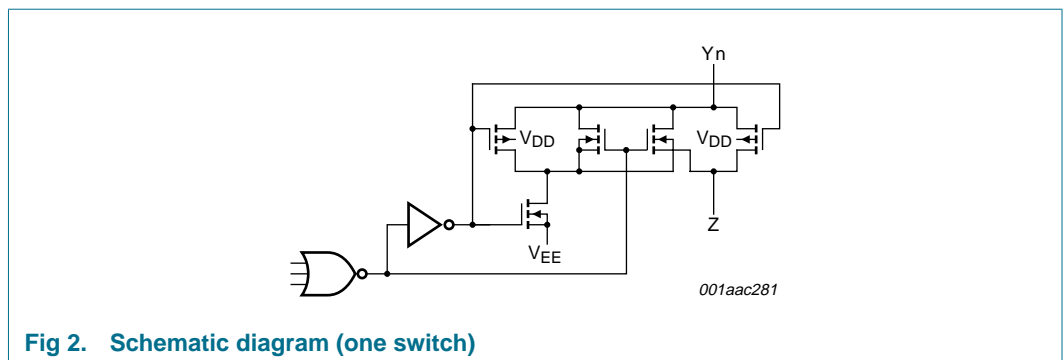


Fig 2. Schematic diagram (one switch)

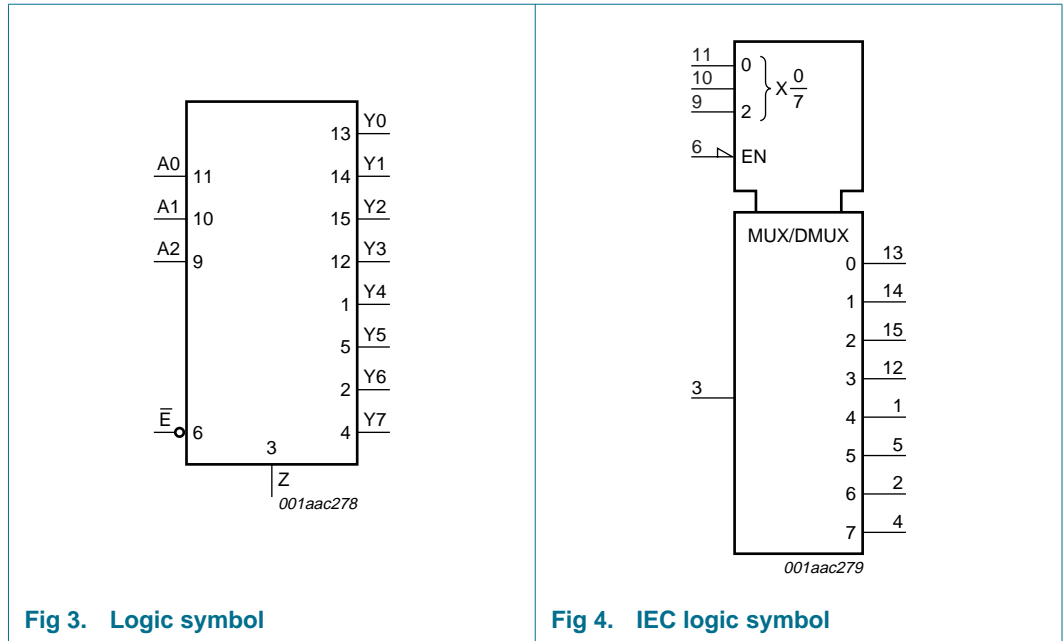


Fig 3. Logic symbol

Fig 4. IEC logic symbol

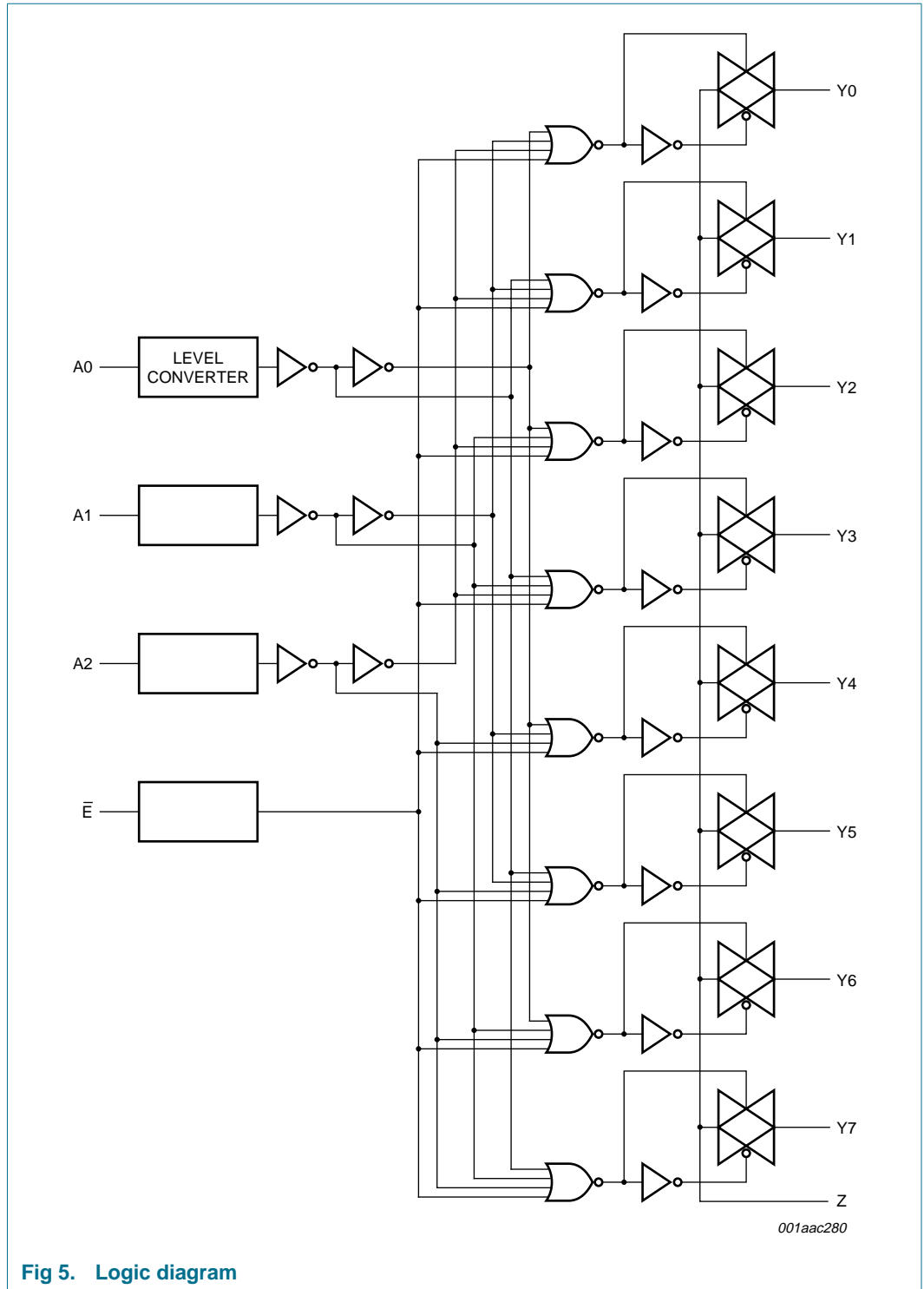
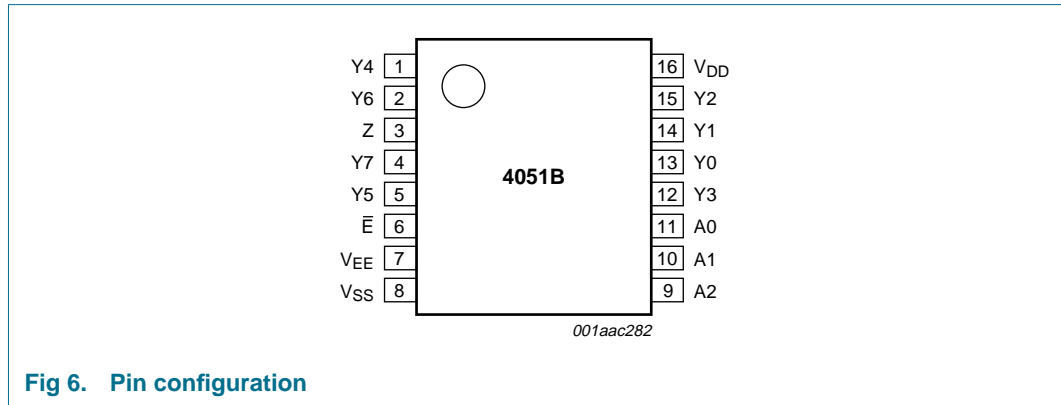


Fig 5. Logic diagram

## 6. Pinning information

### 6.1 Pinning



### 6.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
Y4	1	independent input/output
Y6	2	independent input/output
Z	3	common input/output
Y7	4	independent input/output
Y5	5	independent input/output
$\bar{E}$	6	enable input (active LOW)
$V_{EE}$	7	supply voltage of switches
$V_{SS}$	8	ground (0 V)
A2	9	address input
A1	10	address input
A0	11	address input
Y3	12	independent input/output
Y0	13	independent input/output
Y1	14	independent input/output
Y2	15	independent input/output
$V_{DD}$	16	supply voltage

## 7. Functional description

Table 4: Function table [\[1\]](#)

Inputs				Channel ON
$\bar{E}$	A2	A1	A0	
L	L	L	L	Y0 to Z
L	L	L	H	Y1 to Z
L	L	H	L	Y2 to Z
L	L	H	H	Y3 to Z
L	H	L	L	Y4 to Z
L	H	L	H	Y5 to Z
L	H	H	L	Y6 to Z
L	H	H	H	Y7 to Z
H	X	X	X	-

- [1] H = HIGH voltage level;  
L = LOW voltage level;  
X = don't care.

## 8. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD}$	supply voltage		<a href="#">[1]</a> -0.5	+18	V
$V_{EE}$	supply voltage of switches	referenced to $V_{DD}$	<a href="#">[1]</a> -18	+0.5	V
$V_I$	voltage on any input		-0.5	$V_{DD} + 0.5$	V
I	DC current into any input or output		-	$\pm 10$	mA
$T_{stg}$	storage temperature		-65	+150	°C
$T_{amb}$	ambient temperature		-40	+85	°C
$P_{tot}$	power dissipation	$T_{amb} = -40\text{ °C to }+85\text{ °C}$			
	DIP16		<a href="#">[2]</a> -	700	mW
	SO16, SSOP16 and TSSOP16		<a href="#">[2]</a> -	500	mW
$P_o$	power dissipation per output		-	100	mW

- [1] To avoid drawing  $V_{DD}$  current out of terminal Z, when switch current flows into terminals Y, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal Z, no  $V_{DD}$  current will flow out of terminals Y, in this case there is no limit for the voltage drop across the switch, but the voltages at Y and Z may not exceed  $V_{DD}$  or  $V_{EE}$ .
- [2] For DIP16 packages: above 70 °C, derate linearly with 12 mW/K.  
For SO16 packages: above 70 °C, derate linearly with 8 mW/K.  
For SSOP16 and TSSOP16 packages: above 60 °C, derate linearly with 5.5 mW/K.

## 9. Static characteristics

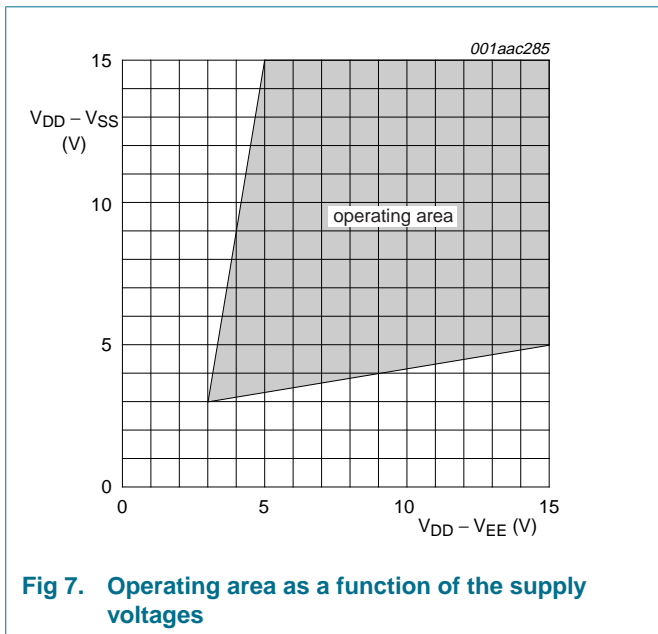
**Table 6: Static characteristics**

$V_{SS} = 0\text{ V}$ ; unless otherwise specified

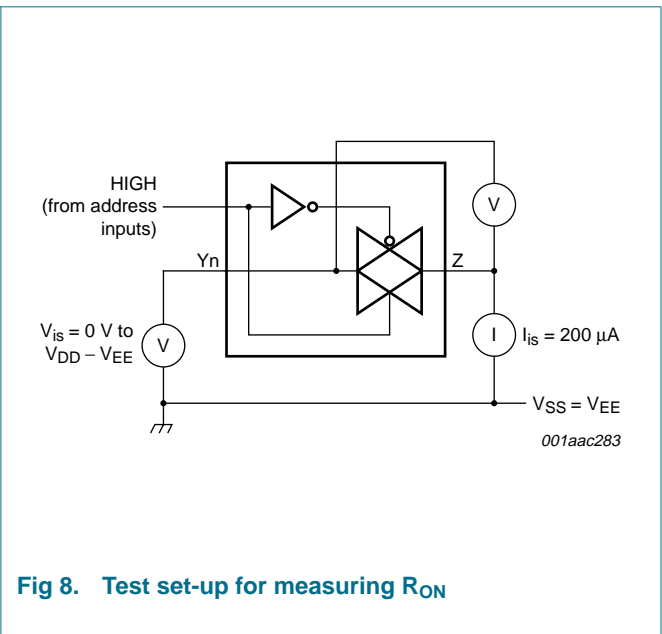
Symbol	Parameter	Conditions	$T_{amb} = -40\text{ °C}$		$T_{amb} = 25\text{ °C}$		$T_{amb} = 85\text{ °C}$		Unit
			Min	Max	Min	Max	Min	Max	
$I_{DD}$	quiescent device current	all valid input combinations; $V_I = V_{SS}$ or $V_{DD}$ ; $I_O = 0\text{ A}$							
		$V_{DD} = 5\text{ V}$	-	20	-	20	-	150	$\mu\text{A}$
		$V_{DD} = 10\text{ V}$	-	40	-	40	-	300	$\mu\text{A}$
		$V_{DD} = 15\text{ V}$	-	80	-	80	-	600	$\mu\text{A}$
$V_{IL}$	LOW-level input voltage	$ I_O  < 1\text{ }\mu\text{A}$							
		$V_O = 0.5\text{ V}$ or $4.5\text{ V}$ ; $V_{DD} = 5\text{ V}$	-	1.5	-	1.5	-	1.5	V
		$V_O = 1.0\text{ V}$ or $9.0\text{ V}$ ; $V_{DD} = 10\text{ V}$	-	3.0	-	3.0	-	3.0	V
		$V_O = 1.5\text{ V}$ or $13.5\text{ V}$ ; $V_{DD} = 15\text{ V}$	-	4.0	-	4.0	-	4.0	V
$V_{IH}$	HIGH-level input voltage	$ I_O  < 1\text{ }\mu\text{A}$							
		$V_O = 0.5\text{ V}$ or $4.5\text{ V}$ ; $V_{DD} = 5\text{ V}$	3.5	-	3.5	-	3.5	-	V
		$V_O = 1.0\text{ V}$ or $9.0\text{ V}$ ; $V_{DD} = 10\text{ V}$	7.0	-	7.0	-	7.0	-	V
		$V_O = 1.5\text{ V}$ or $13.5\text{ V}$ ; $V_{DD} = 15\text{ V}$	11.0	-	11.0	-	11.0	-	V
$I_{LI}$	Input leakage current	$V_I = 0\text{ V}$ or $15\text{ V}$ ; $V_{DD} = 15\text{ V}$	-	0.3	-	0.3	-	1.0	$\mu\text{A}$
$I_{OZ}$	3-state output leakage current	$V_{DD} = 15\text{ V}$							
		output returned to $V_{DD}$	-	1.6	-	1.6	-	12.0	$\mu\text{A}$
		output returned to $V_{SS}$	-	-1.6	-	-1.6	-	-12.0	$\mu\text{A}$
$C_i$	input capacitance digital inputs		-	-	-	7.5	-	-	pF

**Table 7: Static characteristics for  $R_{ON}$**   
 $T_{amb} = 25^{\circ}C$ ;  $R_{ON}$  test conditions see [Figure 8](#)

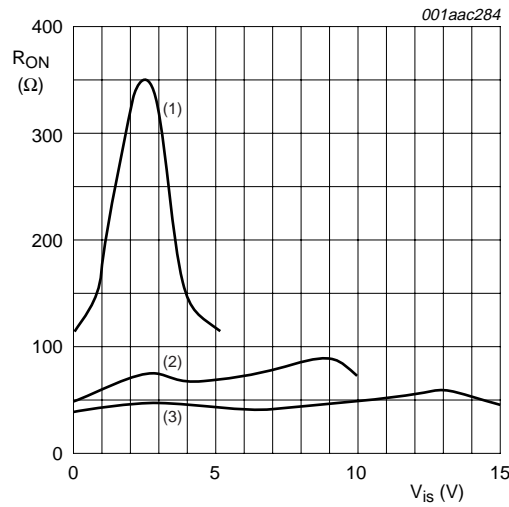
Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
$R_{ON}$	ON resistance	$V_{is} = 0\text{ V to }V_{DD} - V_{EE}$					
		$V_{DD} - V_{EE} = 5\text{ V}$	-	350	2500	$\Omega$	
		$V_{DD} - V_{EE} = 10\text{ V}$	-	80	245	$\Omega$	
		$V_{DD} - V_{EE} = 15\text{ V}$	-	60	175	$\Omega$	
		$V_{is} = 0\text{ V}$					
		$V_{DD} - V_{EE} = 5\text{ V}$	-	115	340	$\Omega$	
		$V_{DD} - V_{EE} = 10\text{ V}$	-	50	160	$\Omega$	
		$V_{DD} - V_{EE} = 15\text{ V}$	-	40	115	$\Omega$	
		$V_{is} = V_{DD} - V_{EE}$					
		$V_{DD} - V_{EE} = 5\text{ V}$	-	120	365	$\Omega$	
		$V_{DD} - V_{EE} = 10\text{ V}$	-	65	200	$\Omega$	
		$V_{DD} - V_{EE} = 15\text{ V}$	-	50	155	$\Omega$	
$\Delta R_{ON}$	ON resistance difference between any two channels	$V_{is} = 0\text{ V to }V_{DD} - V_{EE}$					
		$V_{DD} - V_{EE} = 5\text{ V}$	-	25	-	$\Omega$	
		$V_{DD} - V_{EE} = 10\text{ V}$	-	10	-	$\Omega$	
		$V_{DD} - V_{EE} = 15\text{ V}$	-	5	-	$\Omega$	
$I_{L(OFF)}$	OFF-state leakage current	$V_{SS} = V_{EE}$ ; $V_{DD} - V_{EE} = 15\text{ V}$					
		all channels OFF; $\bar{E}$ at $V_{DD}$	-	-	1000	nA	
		any channel; $\bar{E}$ at $V_{SS}$	-	-	200	nA	



**Fig 7. Operating area as a function of the supply voltages**



**Fig 8. Test set-up for measuring  $R_{ON}$**



$I_{is} = 200 \mu A; V_{SS} = V_{EE} = 0 V.$

- (1)  $V_{DD} = 5 V.$
- (2)  $V_{DD} = 10 V.$
- (3)  $V_{DD} = 15 V.$

Fig 9. Typical  $R_{ON}$  as a function of input voltage

## 10. Dynamic characteristics

Table 8: Dynamic characteristics

$V_{EE} = V_{SS} = 0 V; R_L = 10 k\Omega; C_L = 50 pF; T_{amb} = 25 ^\circ C; input transition times \le 20 ns; test circuit see Figure 13.$

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{PHL}, t_{PLH}$	propagation delay Z to $Y_n$ or $Y_n$ to Z	$\bar{E} = V_{SS}; V_{is} = V_{DD}$ (square-wave); see Figure 10	[1]			
		$V_{DD} = 5 V$	-	15	30	ns
		$V_{DD} = 10 V$	-	5	10	ns
		$V_{DD} = 15 V$	-	5	10	ns
$t_{PHL}$	HIGH to LOW propagation delay An to Z or An to $Y_n$	$\bar{E} = V_{SS}; A_n = V_{DD}$ (square-wave); $V_{is} = V_{EE}$ ; see Figure 11	[1] [2]			
		$V_{DD} = 5 V$	-	150	300	ns
		$V_{DD} = 10 V$	-	60	120	ns
		$V_{DD} = 15 V$	-	45	90	ns
$t_{PLH}$	LOW to HIGH propagation delay An to Z or An to $Y_n$	$\bar{E} = V_{SS}; A_n = V_{DD}$ (square-wave); $V_{is} = V_{DD}$ ; see Figure 11	[1] [2]			
		$V_{DD} = 5 V$	-	150	300	ns
		$V_{DD} = 10 V$	-	65	130	ns
		$V_{DD} = 15 V$	-	45	90	ns

**Table 8: Dynamic characteristics ...continued** $V_{EE} = V_{SS} = 0\text{ V}$ ;  $R_L = 10\text{ k}\Omega$ ;  $C_L = 50\text{ pF}$ ;  $T_{amb} = 25\text{ }^\circ\text{C}$ ; input transition times  $\leq 20\text{ ns}$ ; test circuit see [Figure 13](#).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{PHZ}$	output disable time HIGH to OFF for $\bar{E}$ to Z or $\bar{E}$ to $Y_n$	$\bar{E} = V_{DD}$ (square wave); $V_{is} = V_{DD}$ ; see <a href="#">Figure 12</a> <span style="float:right">[1]</span>				
		$V_{DD} = 5\text{ V}$	-	120	240	ns
		$V_{DD} = 10\text{ V}$	-	90	180	ns
		$V_{DD} = 15\text{ V}$	-	85	170	ns
$t_{PLZ}$	output disable time LOW to OFF for $\bar{E}$ to Z or $\bar{E}$ to $Y_n$	$\bar{E} = V_{DD}$ (square wave); $V_{is} = V_{EE}$ ; see <a href="#">Figure 12</a> <span style="float:right">[1]</span>				
		$V_{DD} = 5\text{ V}$	-	145	290	ns
		$V_{DD} = 10\text{ V}$	-	120	240	ns
		$V_{DD} = 15\text{ V}$	-	115	230	ns
$t_{PZH}$	output enable times OFF to HIGH or LOW for $\bar{E}$ to Z or $\bar{E}$ to $Y_n$	$\bar{E} = V_{DD}$ (square wave); $V_{is} = V_{DD}$ ; see <a href="#">Figure 12</a> <span style="float:right">[1]</span>				
		$V_{DD} = 5\text{ V}$	-	140	280	ns
		$V_{DD} = 10\text{ V}$	-	55	110	ns
		$V_{DD} = 15\text{ V}$	-	40	80	ns
$t_{PZL}$	output enable times OFF to HIGH or LOW for $\bar{E}$ to Z or $\bar{E}$ to $Y_n$	$\bar{E} = V_{DD}$ (square wave); $V_{is} = V_{EE}$ ; see <a href="#">Figure 12</a> <span style="float:right">[1]</span>				
		$V_{DD} = 5\text{ V}$	-	140	280	ns
		$V_{DD} = 10\text{ V}$	-	55	110	ns
		$V_{DD} = 15\text{ V}$	-	40	80	ns
$P_D$	dynamic power dissipation		[3]	-	-	-

[1]  $V_{is}$  is the input voltage at a  $Y_n$  or Z terminal, whichever is assigned as input.  $V_{os}$  is the output voltage at a  $Y_n$  or Z terminal, whichever is assigned as output.

[2] The temperature coefficient for propagation delays is 0.35 %/°C.

[3] Dynamic power dissipation  $P_D$  can be calculated with the following formulae ( $P_D$  in  $\mu\text{W}$ ):

for  $V_{DD} = 5\text{ V}$ ,  $P_D = 1000 \times f_i + \Sigma (f_o \times C_L) \times V_{DD}^2$ ;

for  $V_{DD} = 10\text{ V}$ ,  $P_D = 5500 \times f_i + \Sigma (f_o \times C_L) \times V_{DD}^2$ ;

for  $V_{DD} = 15\text{ V}$ ,  $P_D = 15000 \times f_i + \Sigma (f_o \times C_L) \times V_{DD}^2$ , where:

$f_i$  = input frequency in MHz;

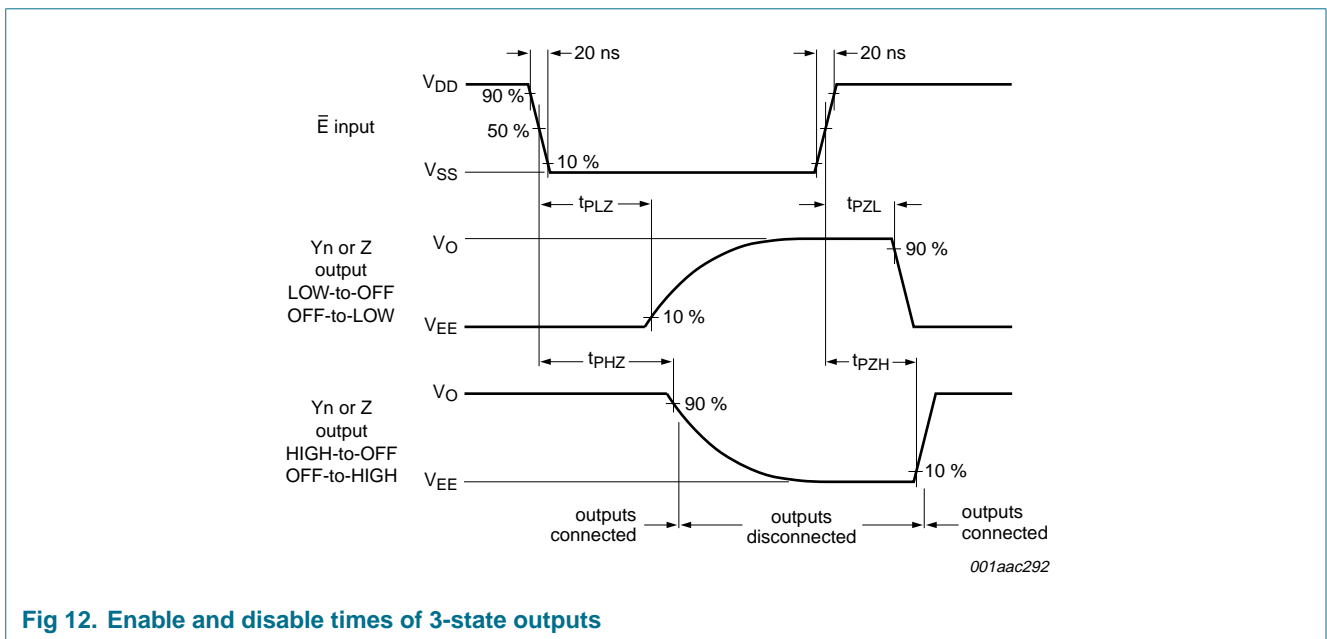
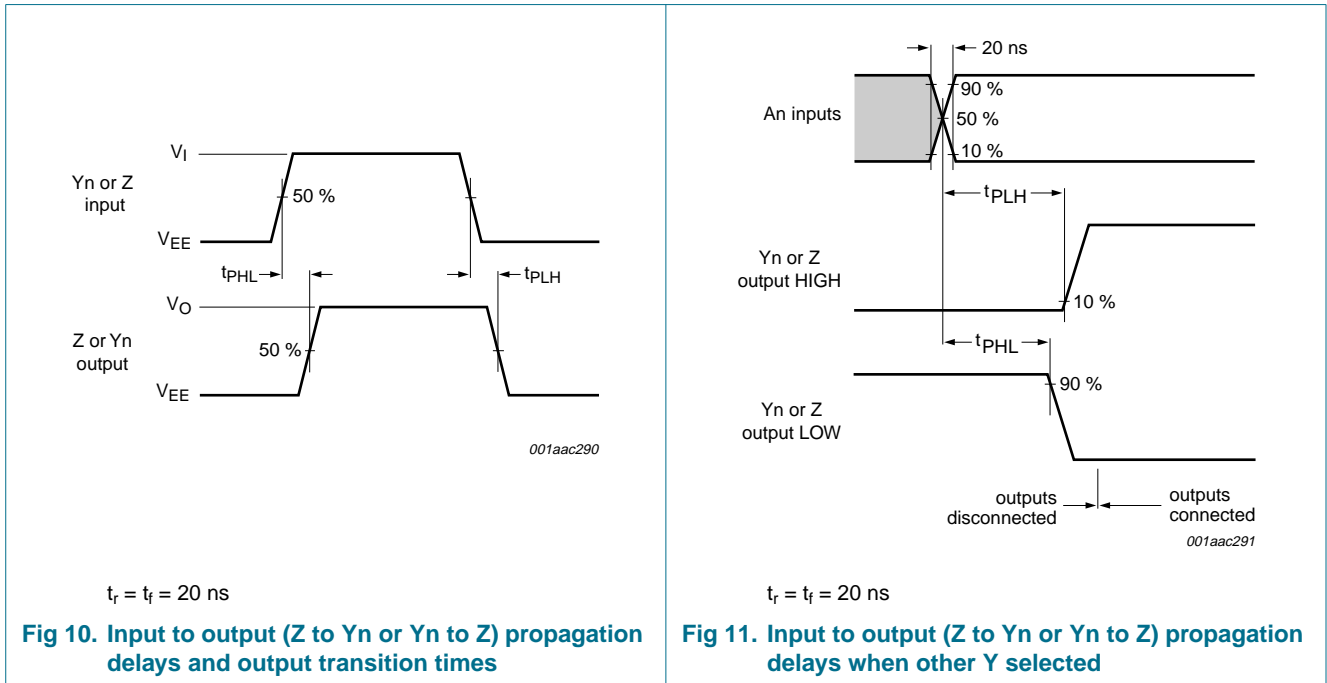
$f_o$  = output frequency in MHz;

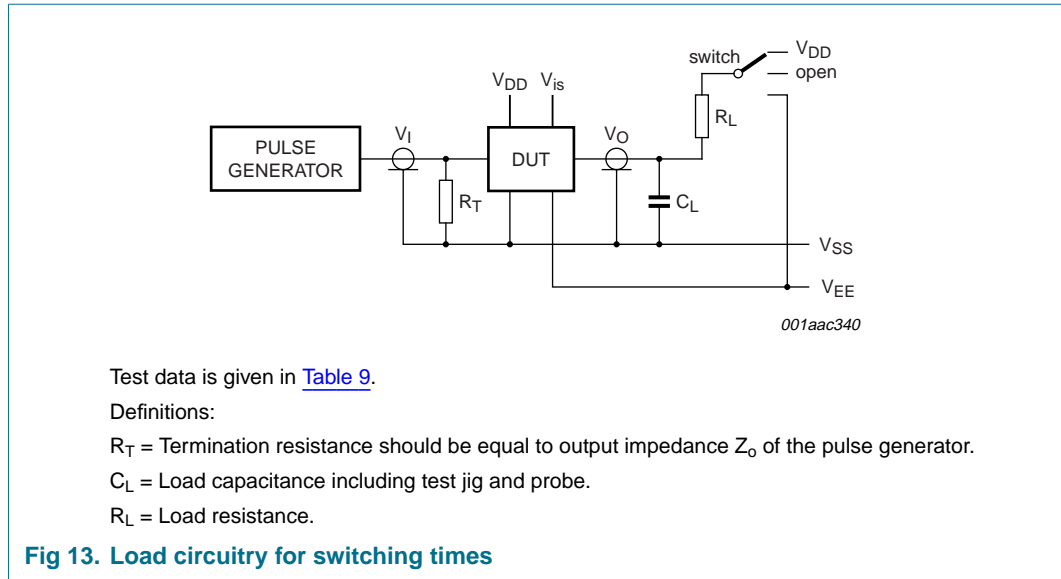
$C_L$  = output load capacitance in pF;

$V_{DD}$  = supply voltage in V;

$\Sigma(C_L \times f_o)$  = sum of the outputs.

11. Waveforms





**Table 9: Test data**

Test	Input		Load		Switch
	$V_{is}$	$t_r, t_f$	$C_L$	$R_L$	
$t_{PHL}$	$V_{EE}$	20 ns	50 pF	10 k $\Omega$	$V_{DD}$
$t_{PLH}$	$V_{DD}$	20 ns	50 pF	10 k $\Omega$	$V_{EE}$
$t_{PZH}, t_{PHZ}$	$V_{DD}$	20 ns	50 pF	10 k $\Omega$	$V_{EE}$
$t_{PZL}, t_{PLZ}$	$V_{EE}$	20 ns	50 pF	10 k $\Omega$	$V_{DD}$
other	pulse	20 ns	50 pF	10 k $\Omega$	open

## 12. Additional dynamic characteristics

**Table 10: Additional dynamic characteristics**

$V_{is} = 0.5V_{DD}(p-p)$  sine-wave and symmetrical.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$d_{sin}$	distortion, sine-wave response	channel ON; $R_L = 10\text{ k}\Omega$ ; $C_L = 15\text{ pF}$ ; $f_{is} = 1\text{ kHz}$ ; see <a href="#">Figure 14</a>				
		$V_{DD} = 5\text{ V}$	-	0.25	-	%
		$V_{DD} = 10\text{ V}$	-	0.04	-	%
		$V_{DD} = 15\text{ V}$	-	0.04	-	%
$f_{ct}$	crosstalk between any two channels	$V_{DD} = 10\text{ V}$	[1] -	1	-	MHz
$V_{ct}$	crosstalk $\bar{E}$ or An to Yn or Z	$R_L = 10\text{ k}\Omega$ ; $C_L = 15\text{ pF}$ ; $\bar{E}$ or An = $V_{DD}$ (square-wave); crosstalk is $ V_{OS} $ (peak value); $V_{DD} = 10\text{ V}$ ; see <a href="#">Figure 15</a>	-	50	-	mV
$f_{OFF}$	OFF-state feed-through	$V_{DD} = 10\text{ V}$	[2] -	1	-	MHz

**Table 10: Additional dynamic characteristics ...continued**

$V_{is} = 0.5V_{DD}(p-p)$  sine-wave and symmetrical.

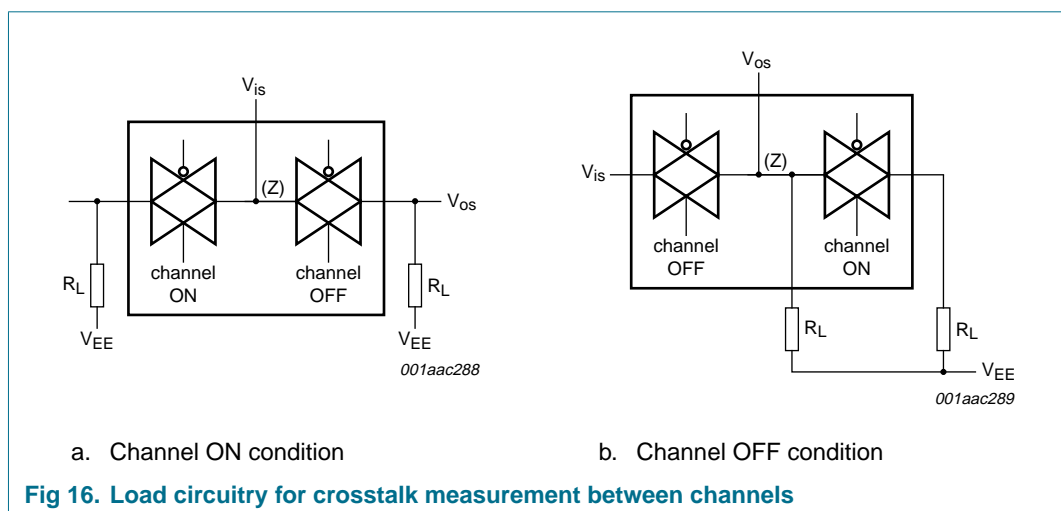
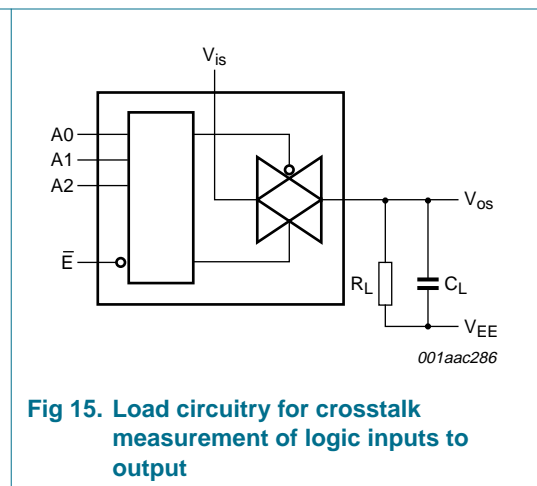
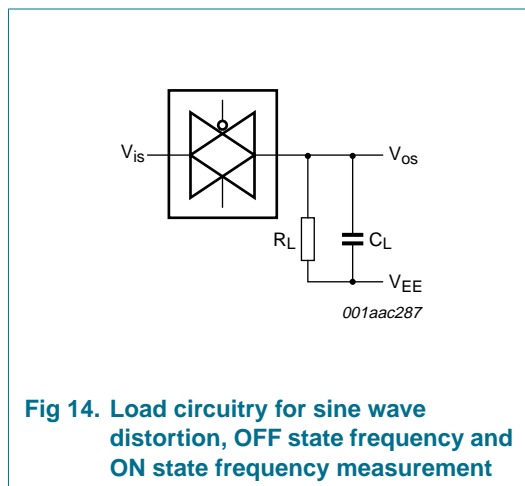
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{ON}$	ON-state frequency response	$V_{DD} = 5\text{ V}$	[3] -	13	-	MHz
		$V_{DD} = 10\text{ V}$	[3] -	40	-	MHz
		$V_{DD} = 15\text{ V}$	[3] -	70	-	MHz

[1]  $R_L = 1\text{ k}\Omega$ ;  $20\log \frac{V_{os}}{V_{is}} = -50\text{ dB}$ ; see [Figure 16](#).

[2]  $R_L = 1\text{ k}\Omega$ ;  $C_L = 5\text{ pF}$ ; channel OFF;  $20\log \frac{V_{os}}{V_{is}} = -50\text{ dB}$ ; see [Figure 14](#).

[3]  $R_L = 1\text{ k}\Omega$ ;  $C_L = 5\text{ pF}$ ; channel ON;  $20\log \frac{V_{os}}{V_{is}} = -3\text{ dB}$ ; see [Figure 14](#).

### 13. Test circuits additional dynamic characteristics



14. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil); long body

SOT38-1

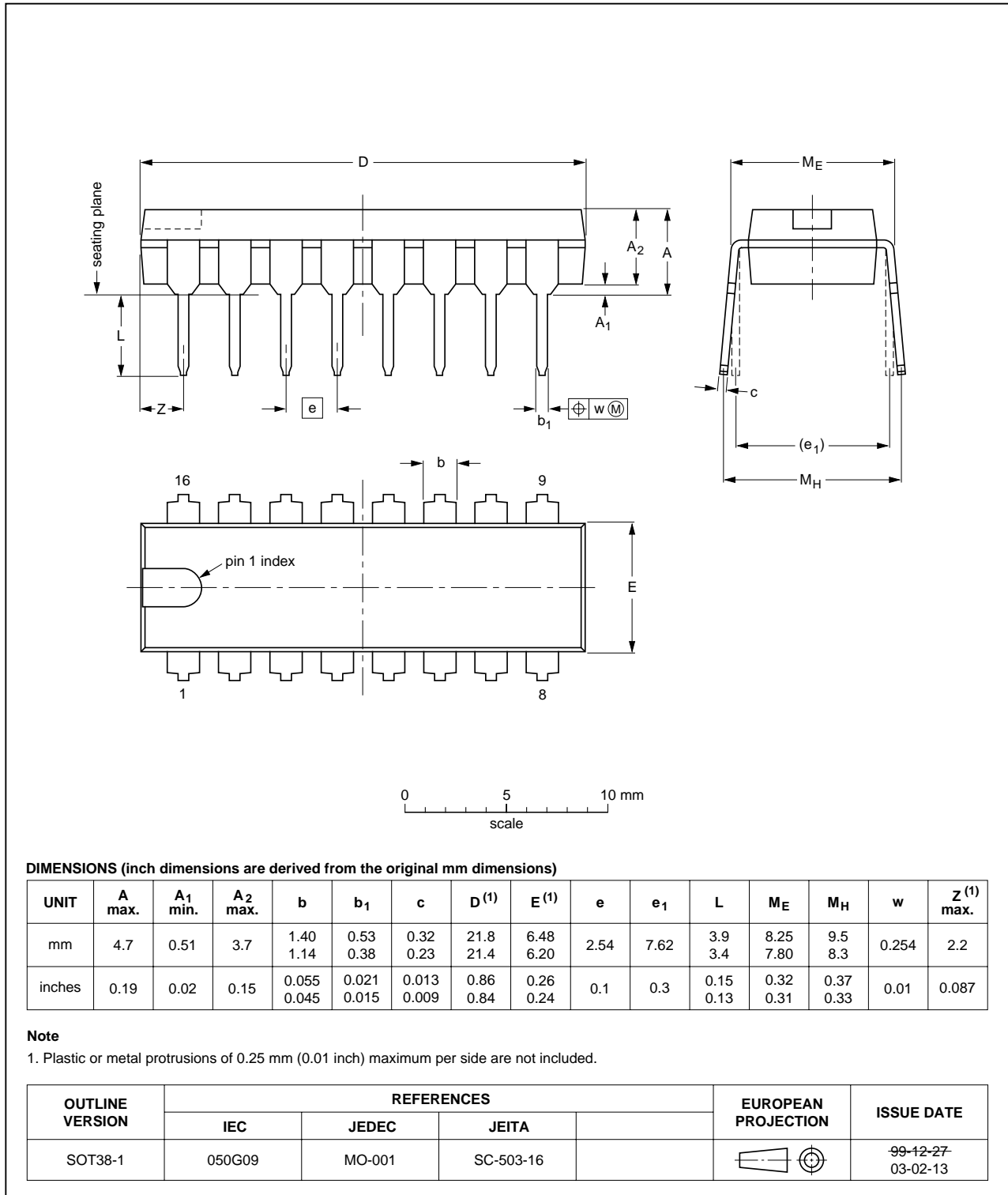


Fig 17. Package outline SOT38-1 (DIP16)

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

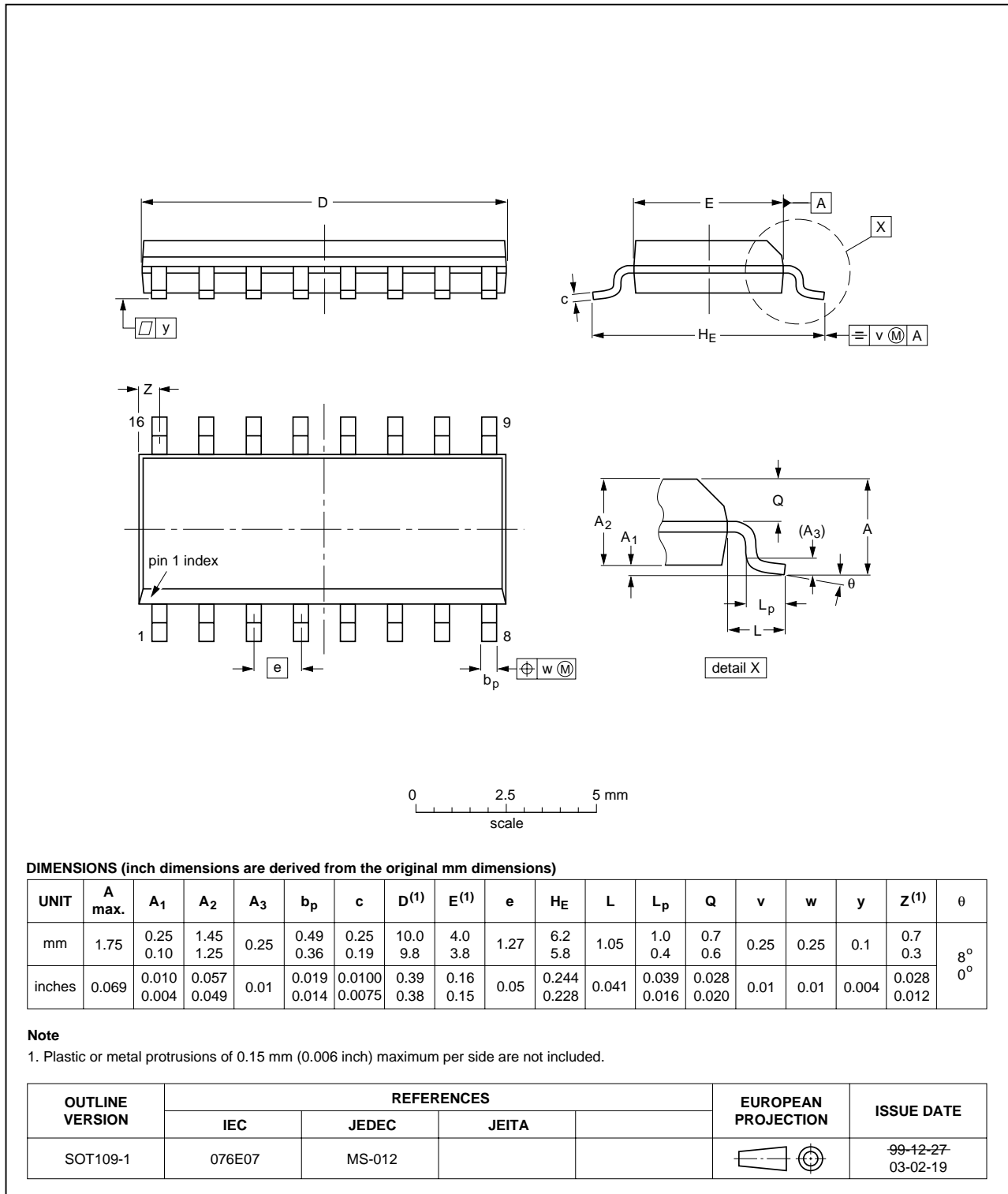


Fig 18. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1

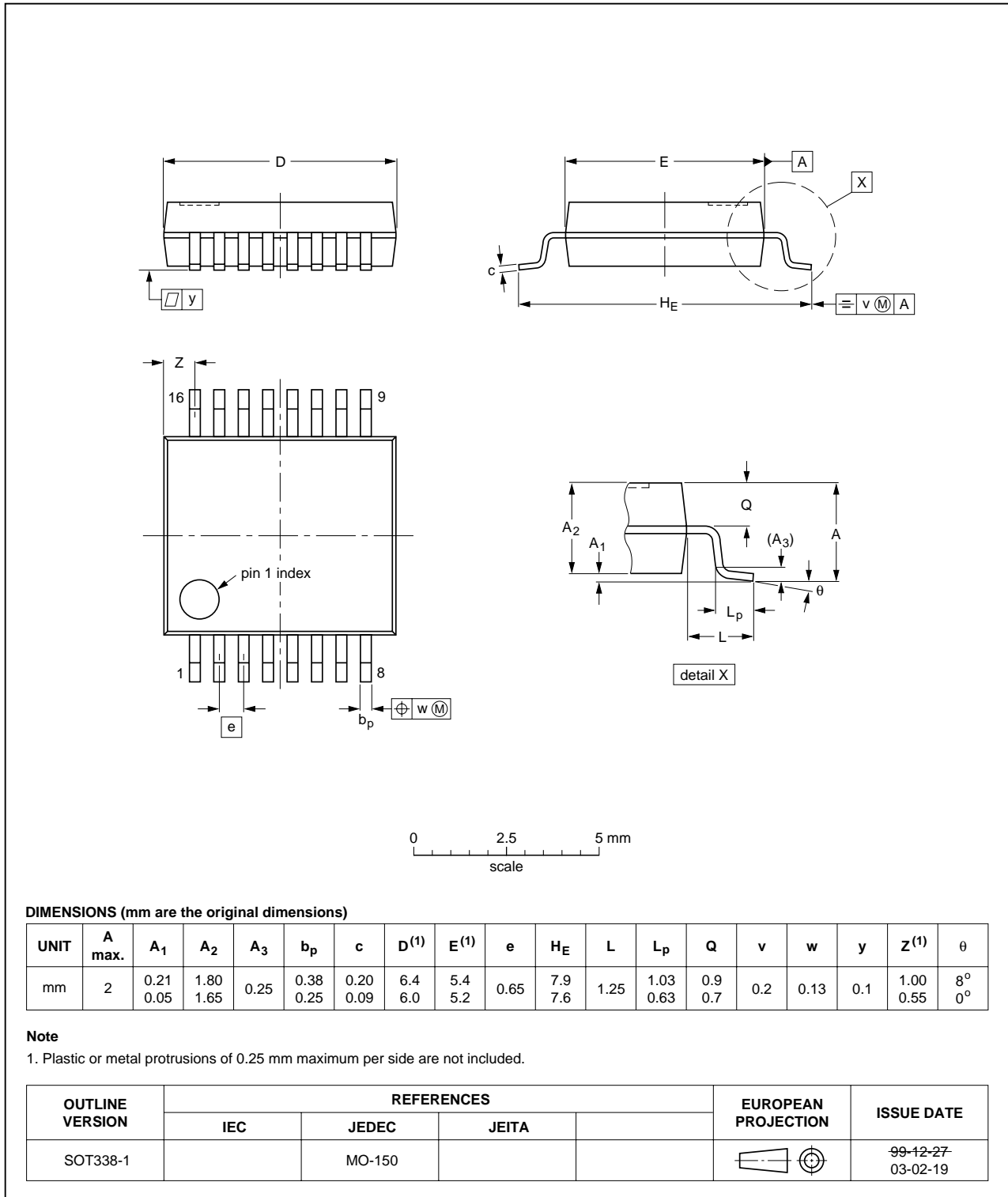


Fig 19. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

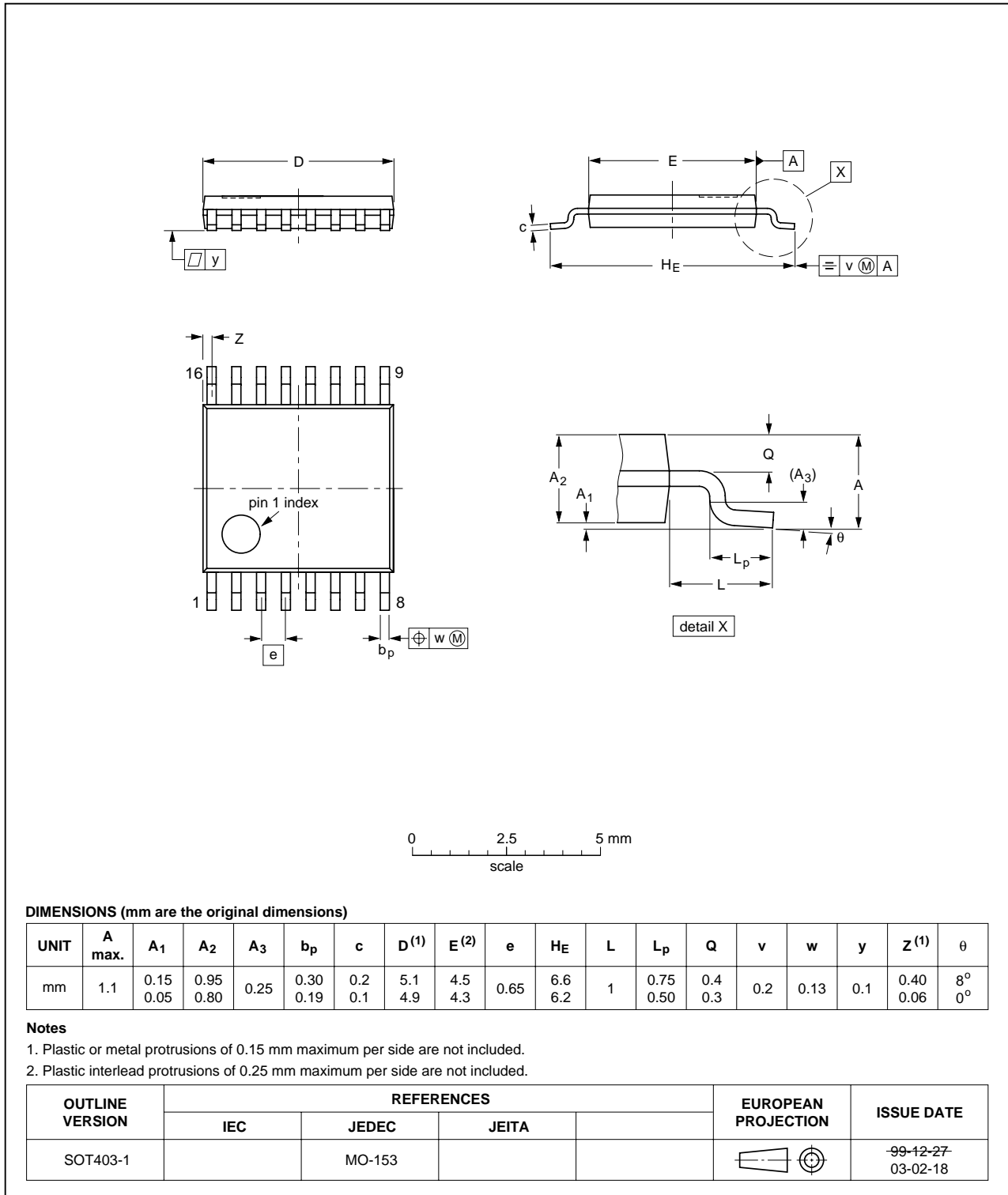


Fig 20. Package outline SOT403-1 (TSSOP16)

## 15. Revision history

Table 11: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
HEF4051B_4	20050112	Product data sheet	-	9397 750 14377	HEF4051B_CNV_3
Modifications:					
					<ul style="list-style-type: none"><li>• The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors.</li><li>• <a href="#">Section 4 "Ordering information"</a>, and <a href="#">Section 14 "Package outline"</a>: Modified to include the SOT338-1 (SSOP16) and SOT403-1 (TSSOP16) packages and to remove the SOT74 (CDIP16) package</li></ul>
HEF4051B_CNV_3	19950101	Product specification	-	-	-

## 16. Data sheet status

Level	Data sheet status <sup>[1]</sup>	Product status <sup>[2]</sup> <sup>[3]</sup>	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

## 17. Definitions

**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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## 19. Contact information

For additional information, please visit: <http://www.semiconductors.philips.com>

For sales office addresses, send an email to: [sales.addresses@www.semiconductors.philips.com](mailto:sales.addresses@www.semiconductors.philips.com)

## 20. Contents

1	General description . . . . .	1
2	Features . . . . .	1
3	Quick reference data . . . . .	2
4	Ordering information . . . . .	2
5	Functional diagram . . . . .	3
6	Pinning information . . . . .	6
6.1	Pinning . . . . .	6
6.2	Pin description . . . . .	6
7	Functional description . . . . .	7
8	Limiting values . . . . .	7
9	Static characteristics . . . . .	8
10	Dynamic characteristics . . . . .	10
11	Waveforms . . . . .	12
12	Additional dynamic characteristics . . . . .	13
13	Test circuits additional dynamic characteristics . . . . .	14
14	Package outline . . . . .	15
15	Revision history . . . . .	19
16	Data sheet status . . . . .	20
17	Definitions . . . . .	20
18	Disclaimers . . . . .	20
19	Contact information . . . . .	20



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