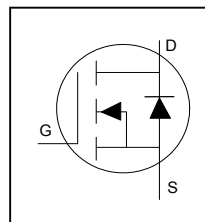


Application

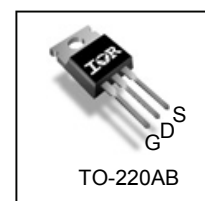
- Optimized for UPS/Inverter Applications
- Low Voltage Power Tools

Benefits

- Best in Class Performance for UPS/Inverter Applications
- Very Low RDS(on) at 4.5V VGS
- Ultra-Low Gate Impedance
- Fully Characterized Avalanche Voltage and Current
- Lead-Free, RoHS Compliant


HEXFET® Power MOSFET

V_{DSS}	30	V
R_{DS(on)} max (@ V _{GS} = 10V)	2.4	mΩ
(@ V _{GS} = 4.5V)	3.2	
Qg (typical)	40	nC
I_D (Silicon Limited)	171 ⑥	A
I_D (Package Limited)	130A	



G	D	S
Gate	Drain	Source

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRLB8314PbF	TO-220AB	Tube	50	IRLB8314PbF

Absolute Maximum Rating

Symbol	Parameter	Max.	Units
V _{GS}	Gate-to-Source Voltage	± 20	V
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V (Silicon Limited)	171 ⑥	A
I _D @ T _C = 100°C	Continuous Drain Current, V _{GS} @ 10V (Silicon Limited)	120	
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V (Package Limited)	130	
I _{DM}	Pulsed Drain Current ①	664	
P _D @ T _C = 25°C	Maximum Power Dissipation	125	W
P _D @ T _C = 100°C	Maximum Power Dissipation	63	W
	Linear Derating Factor	0.83	W/°C
T _J	Operating Junction and	-55 to + 175	°C
T _{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting Torque, 6-32 or M3 Screw	10 lbf·in (1.1 N·m)	

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
R _{θJC}	Junction-to-Case ④	—	1.2	°C/W
R _{θCS}	Case-to-Sink, Flat Greased Surface	0.50	—	
R _{θJA}	Junction-to-Ambient	—	62	

Notes ① through ④ are on page 8

Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	30	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	14	—	mV/ $^\circ\text{C}$	Reference to 25°C , $I_D = 1\text{mA}$ ①
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	1.9	2.4	m Ω	$V_{GS} = 10V, I_D = 68A$ ③
		—	2.6	3.2		$V_{GS} = 4.5V, I_D = 68A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	1.2	1.7	2.2	V	$V_{DS} = V_{GS}, I_D = 100\mu A$
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	-7.0	—	mV/ $^\circ\text{C}$	
I_{DSS}	Drain-to-Source Leakage Current	—	—	1.0	μA	$V_{DS} = 24V, V_{GS} = 0V$
		—	—	150		$V_{DS} = 24V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$
g_{fs}	Forward Transconductance	307	—	—	S	$V_{DS} = 15V, I_D = 68A$
Q_g	Total Gate Charge	—	40	60	nC	$V_{DS} = 15V$ $V_{GS} = 4.5V$ $I_D = 68A$
Q_{gs1}	Pre-V _{th} Gate-to-Source Charge	—	6.8	—		
Q_{gs2}	Post-V _{th} Gate-to-Source Charge	—	13	—		
Q_{gd}	Gate-to-Drain Charge	—	8.7	—		
Q_{godr}	Gate Charge Overdrive	—	11.5	—		
Q_{sw}	Switch Charge ($Q_{gs2} + Q_{gd}$)	—	21.7	—		
R_G	Gate Resistance	—	1.7	—	Ω	
$t_{d(on)}$	Turn-On Delay Time	—	19	—	ns	$V_{DD} = 15V$ $I_D = 68A$ $R_G = 1.8\Omega$ $V_{GS} = 4.5V$ ③
t_r	Rise Time	—	142	—		
$t_{d(off)}$	Turn-Off Delay Time	—	32	—		
t_f	Fall Time	—	72	—		
C_{iss}	Input Capacitance	—	5050	—	pF	$V_{GS} = 0V$ $V_{DS} = 15V$ $f = 1.0\text{MHz}$
C_{oss}	Output Capacitance	—	890	—		
C_{rss}	Reverse Transfer Capacitance	—	500	—		

Avalanche Characteristics

E_{AS} (Thermally limited)	Single Pulse Avalanche Energy ②	180	mJ
E_{AS} (tested)	Single Pulse Avalanche Energy Tested Value ⑤	900	
I_{AR}	Avalanche Current ①	68	A
E_{AR}	Repetitive Avalanche Energy ①	12.5	mJ

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode) ①	—	—	171 ⑥	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	664		
V_{SD}	Diode Forward Voltage	—	—	1.0	V	$T_J = 25^\circ\text{C}, I_S = 68A, V_{GS} = 0V$ ③
t_{rr}	Reverse Recovery Time	—	21	31	ns	$T_J = 25^\circ\text{C}, I_F = 68A, V_{DD} = 15V$
Q_{rr}	Reverse Recovery Charge	—	54	81	nC	$di/dt = 430A/\mu s$ ③

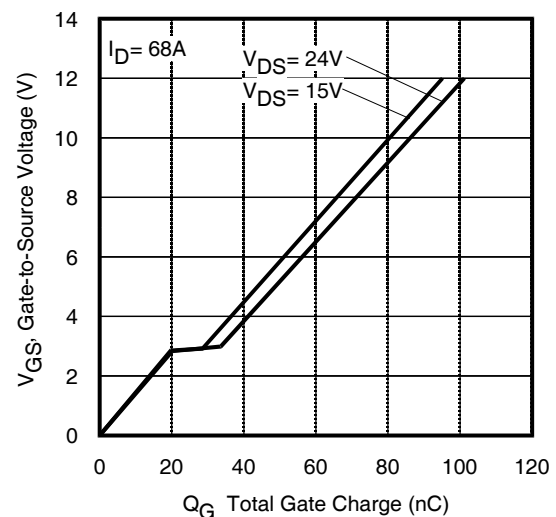
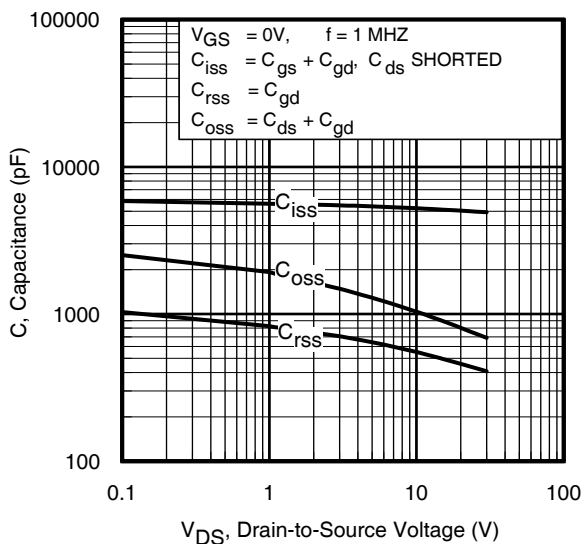
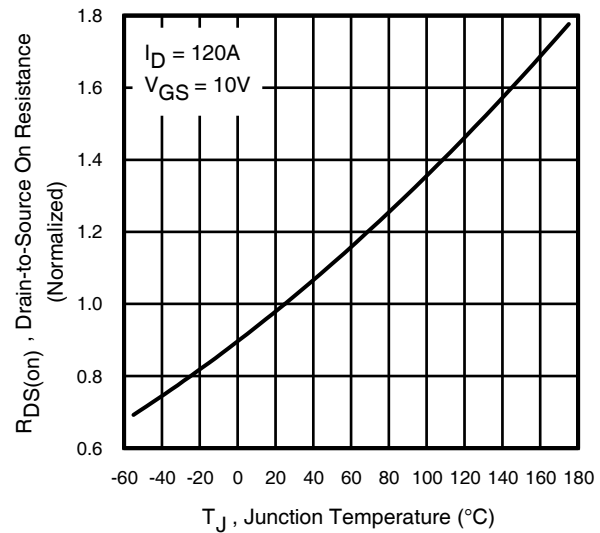
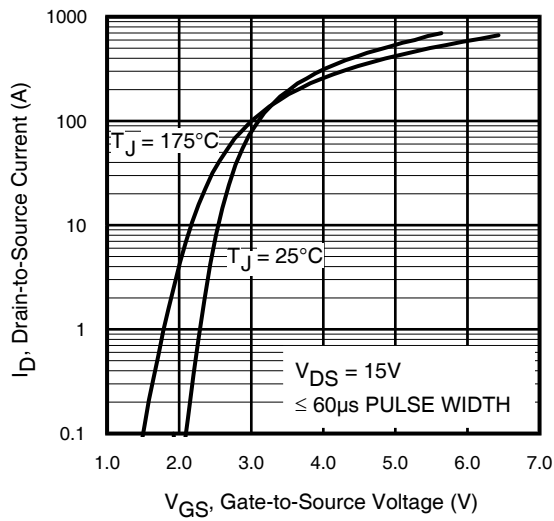
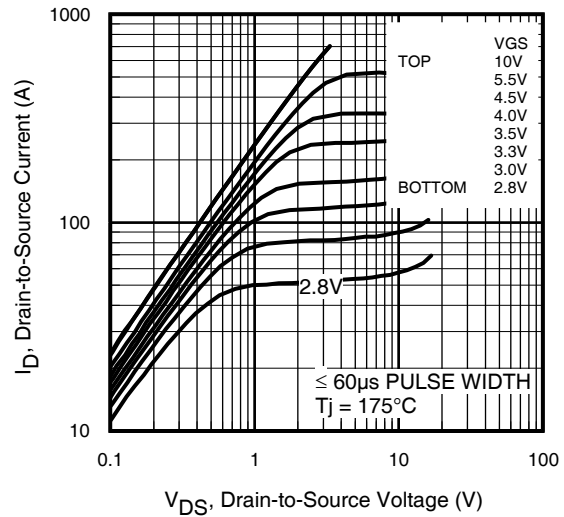
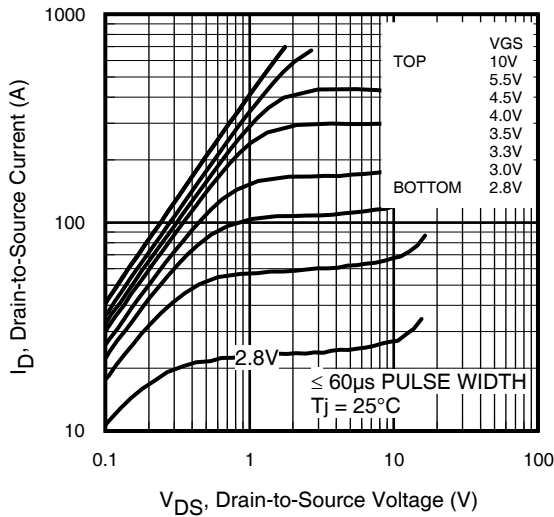
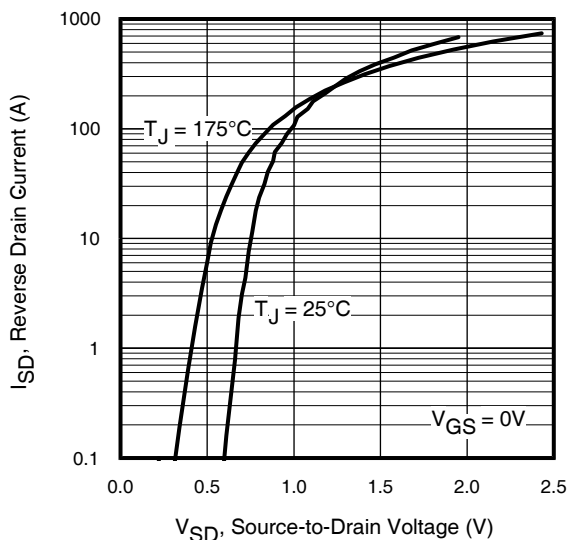
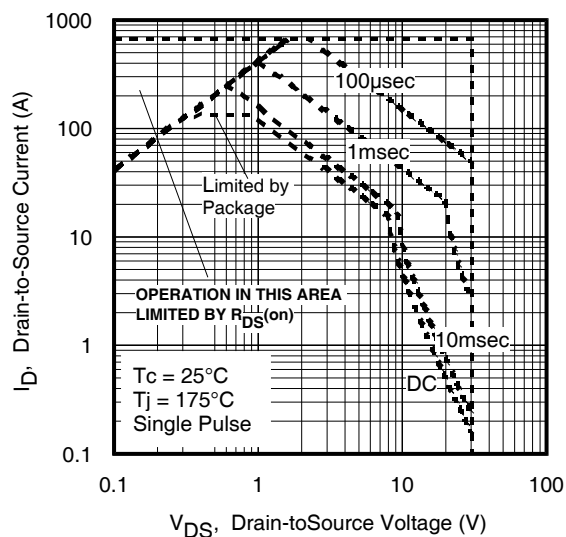
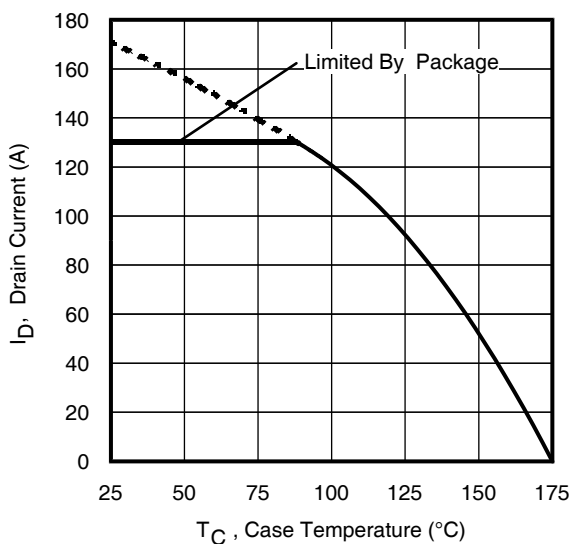
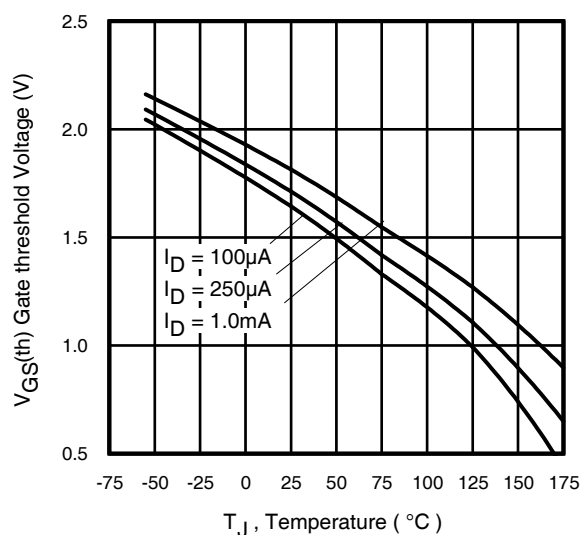
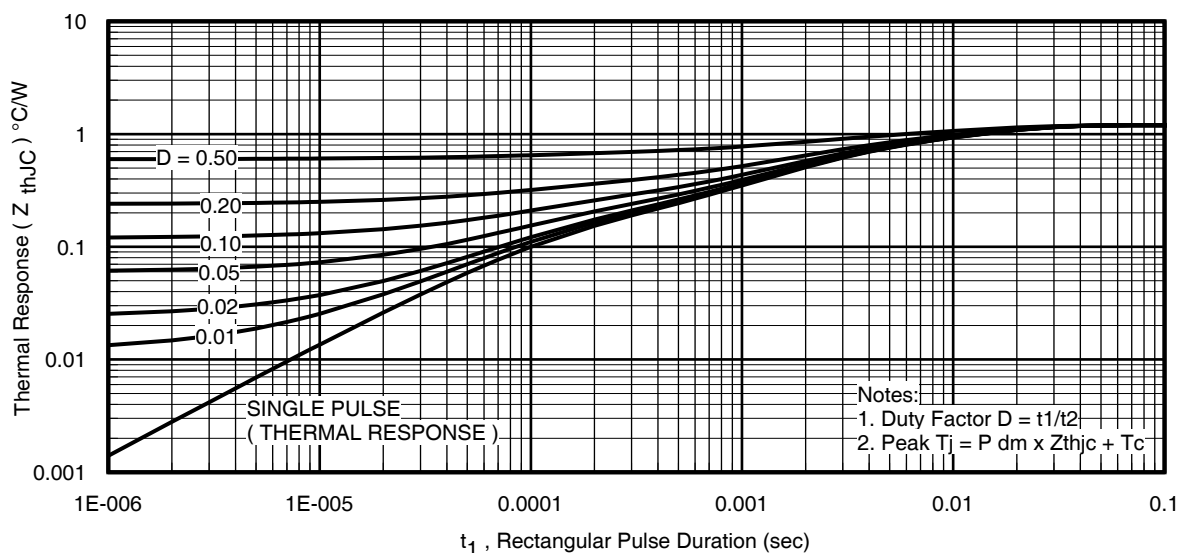


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage


Fig 7. Typical Source-Drain Diode Forward Voltage

Fig 8. Maximum Safe Operating Area

Fig 9. Maximum Drain Current vs. Case Temperature

Fig 10. Threshold Voltage vs. Temperature

Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

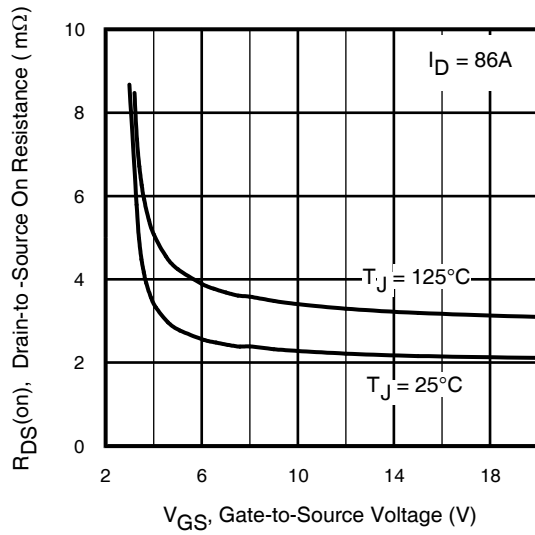


Fig 12. Typical On-Resistance vs. Gate Voltage

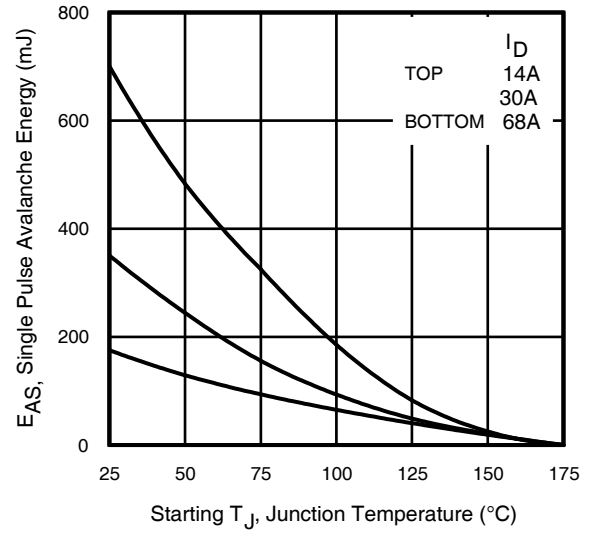


Fig 13. Maximum Avalanche Energy vs. Drain Current

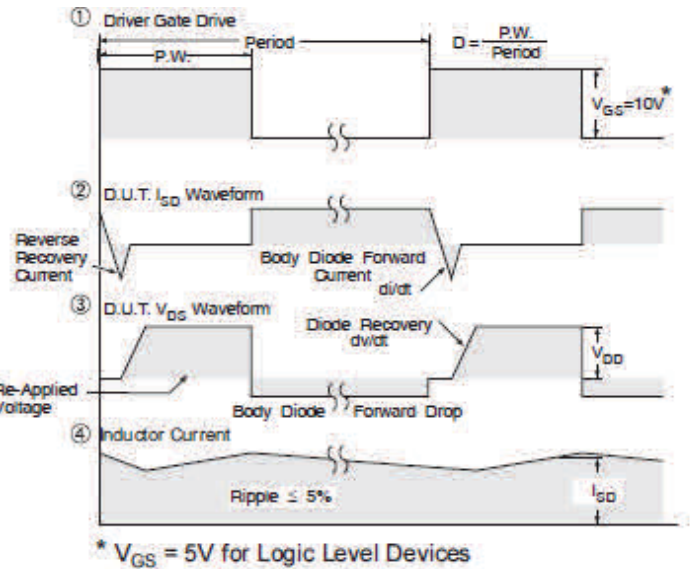
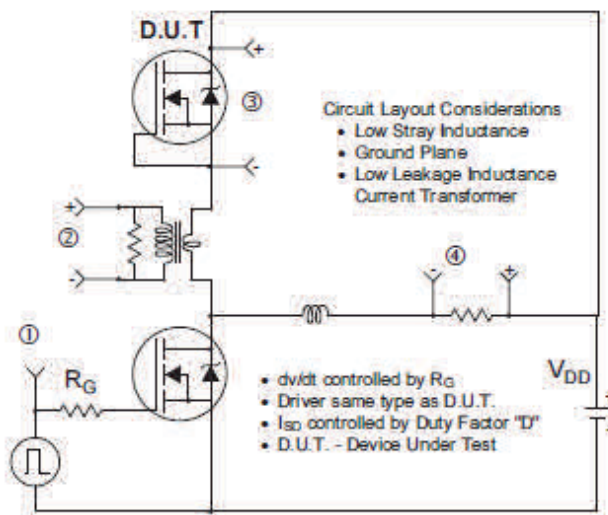


Fig 14. Peak Diode Recovery dV/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

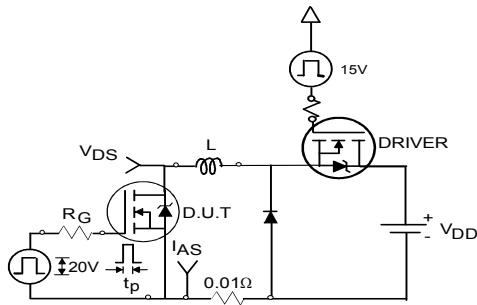


Fig 15a. Unclamped Inductive Test Circuit

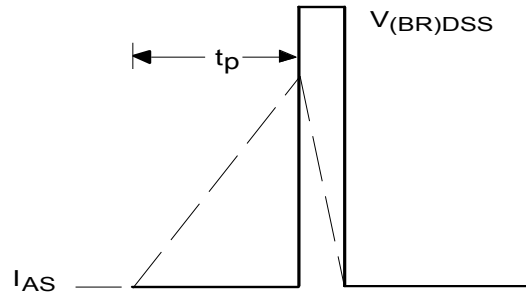


Fig 15b. Unclamped Inductive Waveforms

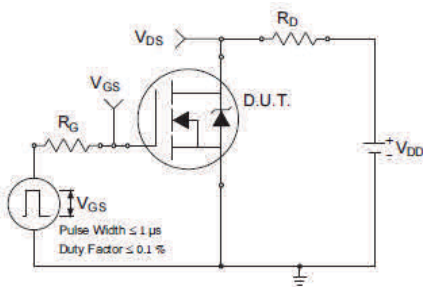


Fig 16a. Switching Time Test Circuit

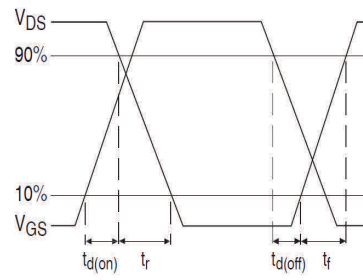


Fig 16b. Switching Time Waveforms

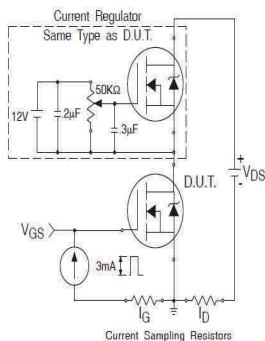


Fig 17a. Gate Charge Test Circuit

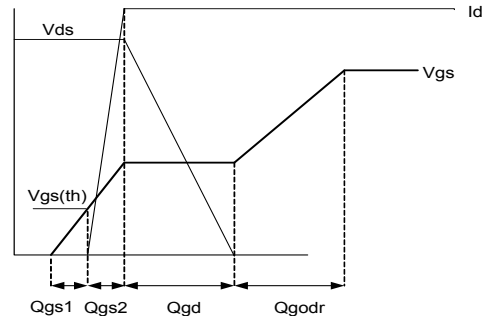
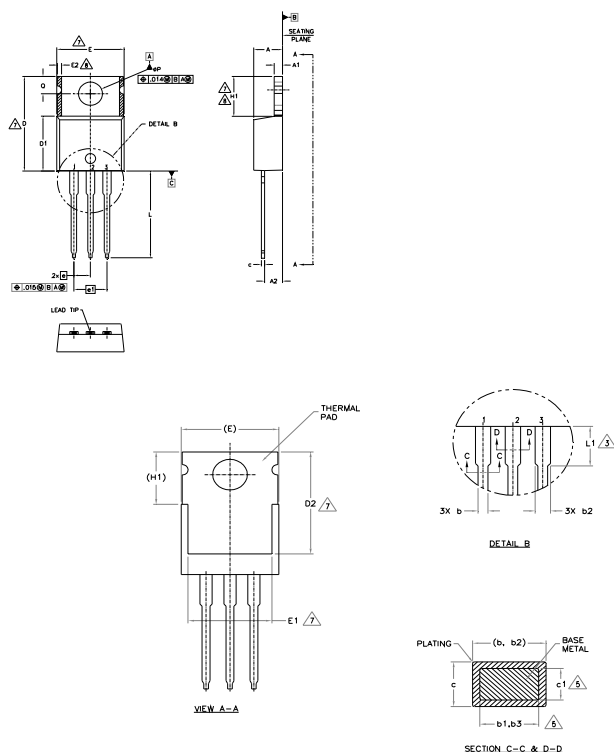


Fig 17b. Gate Charge Waveform

TO-220AB Package Outline (Dimensions are shown in millimeters (inches))

NOTES:

- 1.- DIMENSIONING AND TOLERANCING AS PER ASME Y14.5 M- 1994.
- 2.- DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
- 3.- LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
- 4.- DIMENSION D, D1 & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- 5.- DIMENSION b1, b3 & c1 APPLY TO BASE METAL ONLY.
- 6.- CONTROLLING DIMENSION : INCHES.
- 7.- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS E,H1,D2 & E1
- 8.- DIMENSION E2 X H1 DEFINE A ZONE WHERE STAMPING AND SINGULATION IRREGULARITIES ARE ALLOWED.
- 9.- OUTLINE CONFORMS TO JEDEC TO-220, EXCEPT A2 (max.) AND D2 (min.) WHERE DIMENSIONS ARE DERIVED FROM THE ACTUAL PACKAGE OUTLINE.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	3.56	4.83	.140	.190	
A1	0.51	1.40	.020	.055	
A2	2.03	2.92	.080	.115	
b	0.38	1.01	.015	.040	
b1	0.38	0.97	.015	.038	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.36	0.61	.014	.024	
c1	0.36	0.56	.014	.022	5
D	14.22	16.51	.560	.650	4
D1	8.38	9.02	.330	.355	
D2	11.68	12.88	.460	.507	7
E	9.65	10.67	.380	.420	4,7
E1	6.86	8.89	.270	.350	7
E2	—	0.76	—	.030	8
e	2.54 BSC		.100 BSC		
e1	5.08 BSC		.200 BSC		
H1	5.84	6.86	.230	.270	7,8
L	12.70	14.73	.500	.580	
L1	3.56	4.06	.140	.160	3
øP	3.54	4.08	.139	.161	
Q	2.54	3.42	.100	.135	

LEAD ASSIGNMENTS
HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE

IGBTs, CoPACK

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER

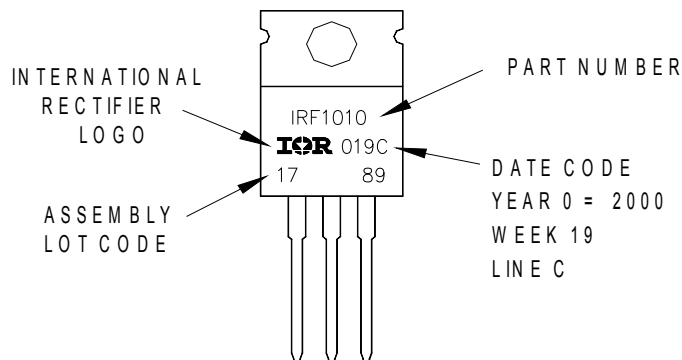
DIODES

- 1.- ANODE
- 2.- CATHODE
- 3.- ANODE

TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010
LOT CODE 1789
ASSEMBLED ON WW 19, 2000
IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position
indicates "Lead - Free"



TO-220AB packages are not recommended for Surface Mount Application.

Qualification Information

Qualification Level	Industrial (per JEDEC JESD47F) †	
Moisture Sensitivity Level	TO-220AB	N/A
RoHS Compliant	Yes	

† Applicable version of JEDEC standard at the time of product release.

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Limited by T_{Jmax} , starting $T_J = 25^{\circ}C$, $L = 0.067mH$, $R_G = 50\Omega$, $I_{AS} = 68A$, $V_{GS} = 10V$.
- ③ Pulse width $\leq 400\mu s$; duty cycle $\leq 2\%$.
- ④ R_{θ} is measured at T_J approximately $90^{\circ}C$.
- ⑤ This value determined from sample failure population, starting $T_J = 25^{\circ}C$, $L = 0.5mH$, $R_G = 50\Omega$, $I_{AS} = 60A$, $V_{GS} = 10V$.
- ⑥ Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 130A. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements. (Refer to AN-1140).

Revision History

Date	Comments
08/04/2016	- Changed datasheet with Infineon logo - all pages. - Corrected package type from "TO-220Pak" to "TO-220AB" on page 1 and page 8. - Updated figure numbers on page 5 & 6. - Added disclaimer on last page.

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