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QA3111N6N

30V Asymmetric Dual N-Channel Power MOSFET

General Description

The QA3111N6N is a high performance trench Dual N-channel asymmetric MOSFET which utilizes extremely high cell density to provide low $R_{DS(on)}$ and gate charge characteristics. It is ideally suited to support synchronous buck converter applications.

The QA3111N6N meets RoHS and Green Product requirements while supporting full function reliability.

Features

- ✓ Advanced high cell density Trench technology
- ✓ Super Low Gate Charge
- ✓ Excellent CdV/dt effect decline
- ✓ Green Device Available

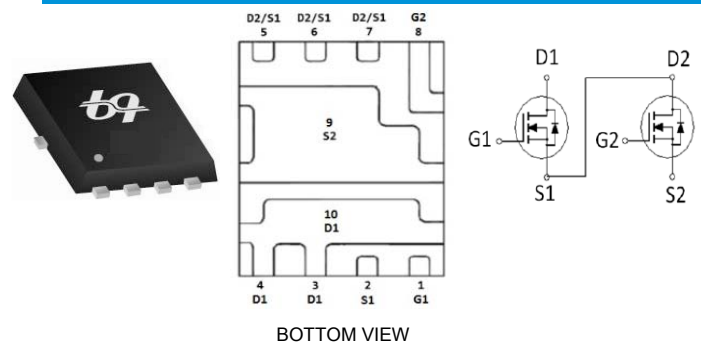
Product Summary

	V_{DS}	$R_{DS(ON)} \max$ ($V_{GS}=10V$)	I_D ($T_C=25^\circ C$)
Die1	30V	5.6m Ω	59A
Die2	30V	1.3m Ω	135A

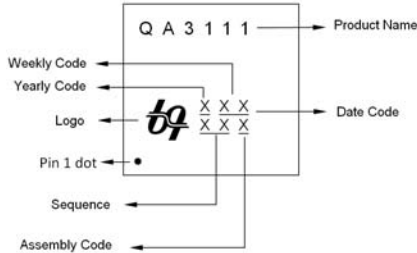
Applications

- ✓ High Frequency Point-of-Load Synchronous Buck Converter for MB/NB/UMPC/VGA
- ✓ Networking DC-DC Power System
- ✓ CCFL Back-light Inverter

Pin Configuration



Ordering Information

Order Number	Package Type	Top Marking
QA3111N6N	DFN5X6	

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Absolute Maximum Ratings

Symbol	Parameter	Rating		Units
		Die1	Die2	
V_{DS}	Drain-Source Voltage	30	30	V
V_{GS}	Gate-Source Voltage	± 20	± 20	V
$I_D@T_C=25^{\circ}C$	Continuous Drain Current, V_{GS} @ 10V ¹	59	135	A
$I_D@T_C=100^{\circ}C$	Continuous Drain Current, V_{GS} @ 10V ¹	37	85	A
$I_D@T_A=25^{\circ}C$	Continuous Drain Current, V_{GS} @ 10V ¹	15	31	A
$I_D@T_A=70^{\circ}C$	Continuous Drain Current, V_{GS} @ 10V ¹	12	25	A
I_{DM}	Pulsed Drain Current ²	118	270	A
EAS	Single Pulse Avalanche Energy ³	58.5	391.6	mJ
I_{AS}	Avalanche Current	34.2	88.5	A
$P_D@T_C=25^{\circ}C$	Total Power Dissipation ⁴	31	40	W
$P_{DSM}@T_A=25^{\circ}C$	Total Power Dissipation ⁴	2	2	W
T_{STG}	Storage Temperature Range	-55 to 150	-55 to 150	$^{\circ}C$
T_J	Operating Junction Temperature Range	-55 to 150	-55 to 150	$^{\circ}C$

Thermal Data

Symbol	Parameter	Die1	Die2	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	62	56	$^{\circ}C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	4	3.1	$^{\circ}C/W$

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Die1 N-Channel Electrical Characteristics

Die1 N-Channel Electrical Characteristics: (T _J =25 °C, unless otherwise noted)						
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	30	--	--	V
ΔBV _{DSS} / ΔT _J	BVDSS Temperature Coefficient	Reference to 25°C, I _D =1mA	--	0.016	--	V/°C
R _{DS(ON)}	Static Drain-Source	V _{GS} =10V, I _D =30A	--	4.3	5.6	mΩ
	On-Resistance ²	V _{GS} =4.5V, I _D =15A	--	6.0	8.4	
V _{GS(th)}	Gate Threshold Voltage	V _{GS} =V _{DS} , I _D =250uA	1.2	--	2.5	V
ΔV _{GS(th)} / ΔT _J	V _{GS(th)} Temperature Coefficient		--	-3.7	--	mV/°C
I _{DSS}	Drain-Source Leakage Current	V _{DS} =24V, V _{GS} =0V	--	--	1	uA
		V _{DS} =24V, V _{GS} =0V, T _J =55°C	--	--	5	
I _{GSS}	Gate-Source Leakage Current	V _{GS} =± 20V, V _{DS} =0V	--	--	±100	nA
g _{fs}	Forward Transconductance	V _{DS} =5V, I _D =30A	--	33	--	S
R _g	Gate Resistance	V _{DS} =0V, V _{GS} =0V, f=1MHz	--	1.6	--	Ω
Q _g	Total Gate Charge	V _{DS} =15V, V _{GS} =10V, I _D =15A	--	14.5	--	nC
Q _g	Total Gate Charge	V _{DS} =15V, V _{GS} =4.5V, I _D =15A	--	6.7	--	nC
Q _{gs}	Gate-Source Charge		--	2.5	--	
Q _{gd}	Gate-Drain Charge		--	2.2	--	
t _{d(on)}	Turn-On Delay Time	V _{DS} =15V, V _{GS} =10V, R _G =3.3Ω, I _D =15A	--	6.5	--	ns
t _r	Rise Time		--	52.1	--	
t _{d(off)}	Turn-Off Delay Time		--	16.0	--	
t _f	Fall Time		--	2.7	--	
C _{iss}	Input Capacitance	V _{DS} =15V, V _{GS} =0V, f=1MHz	--	850	--	pF
C _{oss}	Output Capacitance		--	280	--	
C _{rss}	Reverse Transfer Capacitance		--	18	--	

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Guaranteed Avalanche Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
EAS	Single Pulse Avalanche Energy ⁵	$V_{DD}=25V$, $L=0.1mH$, $I_{AS}=24A$	28.8	--	--	mJ

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current ^{1,6}	$V_G=V_D=0V$, Force Current	--	--	59	A
I_{SM}	Pulsed Source Current ^{2,6}		--	--	118	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V$, $I_S=1A$	--	--	1.2	V
t_{rr}	Reverse Recovery Time	$I_F=15A$, $di/dt=100A/\mu s$, $T_J=25^\circ C$	--	20.7	--	nS
Q_{rr}	Reverse Recovery Charge		--	11.1	--	nC

Note:

1. Test data conducted with surface mount attachment to 1 inch², FR-4 board utilizing 2oz copper
2. Pulse Test. Pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
3. EAS data is a maximum rating. The test condition is $V_{DD}=25V$, $V_{GS}=10V$, $L=0.1mH$
4. The power dissipation is limited by a 150°C maximum junction temperature
5. The Min. value is 100% EAS tested guarantee
6. The data is theoretically the same as I_D and I_{DM} . In real applications, it will be limited by total power

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Die2 N-Channel Electrical Characteristics

Die2 N-Channel Electrical Characteristics: (T _J =25 °C, unless otherwise noted)						
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	30	--	--	V
ΔBV _{DSS} / ΔT _J	BVDSS Temperature Coefficient	Reference to 25°C, I _D =1mA	--	0.016	--	V/°C
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =30A	--	1.0	1.3	mΩ
		V _{GS} =4.5V, I _D =15A	--	1.3	1.8	
V _{GS(th)}	Gate Threshold Voltage	V _{GS} =V _{DS} , I _D =250uA	1.2	--	2.5	V
ΔV _{GS(th)}	V _{GS(th)} Temperature Coefficient		--	-4.9	--	mV/°C
I _{DSS}	Drain-Source Leakage Current	V _{DS} =24V, V _{GS} =0V	--	--	1	uA
		V _{DS} =24V, V _{GS} =0V, T _J =55°C	--	--	5	
I _{GSS}	Gate-Source Leakage Current	V _{GS} =± 20V, V _{DS} =0V	--	--	±100	nA
g _{fs}	Forward Transconductance	V _{DS} =5V, I _D =30A	--	83	--	S
R _g	Gate Resistance	V _{DS} =0V, V _{GS} =0V, f=1MHz	--	0.6	--	Ω
Q _g	Total Gate Charge	V _{DS} =15V, V _{GS} =10V, I _D =15A	--	52.2	--	nC
Q _g	Total Gate Charge	V _{DS} =15V, V _{GS} =4.5V, I _D =15A	--	23.5	--	nC
Q _{gs}	Gate-Source Charge		--	10.8	--	
Q _{gd}	Gate-Drain Charge		--	4.7	--	
t _{d(on)}	Turn-On Delay Time	V _{DS} =15V, V _{GS} =10V, R _G =3.3Ω, I _D =15A	--	11.4	--	ns
t _r	Rise Time		--	46.9	--	
t _{d(off)}	Turn-Off Delay Time		--	35.9	--	
t _f	Fall Time		--	5.9	--	
C _{iss}	Input Capacitance	V _{DS} =15V, V _{GS} =0V, f=1MHz	--	4040	--	pF
C _{oss}	Output Capacitance		--	1310	--	
C _{rss}	Reverse Transfer Capacitance		--	65	--	

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Guaranteed Avalanche Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
EAS	Single Pulse Avalanche Energy ⁵	$V_{DD}=25V$, $L=0.1mH$, $I_{AS}=63A$	198.45	--	--	mJ

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current ^{1,6}	$V_G=V_D=0V$, Force Current	--	--	135	A
I_{SM}	Pulsed Source Current ^{2,6}		--	--	270	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V$, $I_S=1A$	--	--	1.2	V
t_{rr}	Reverse Recovery Time	$I_F=15A$, $di/dt=100A/\mu s$, $T_J=25^\circ C$	--	109	--	nS
Q_{rr}	Reverse Recovery Charge		--	126	--	nC

Note:

1. Test data conducted with surface mount attachment to 1 inch², FR-4 board utilizing 2oz copper
2. Pulse Test. Pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
3. EAS data is a maximum rating. The test condition is $V_{DD}=50V$, $V_{GS}=10V$, $L=0.1mH$
4. The power dissipation is limited by a 150°C maximum junction temperature
5. The Min. value is 100% EAS tested guarantee
6. The data is theoretically the same as I_D and I_{DM} . In real applications, it will be limited by total power

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Die1 Typical Characteristics

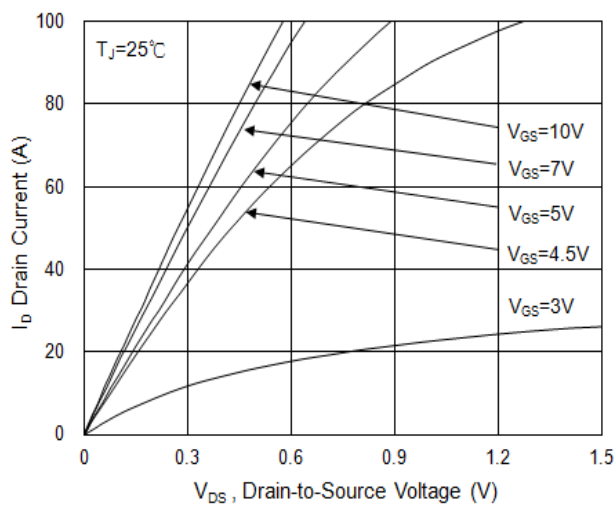


Fig.1: Typical Output Characteristics

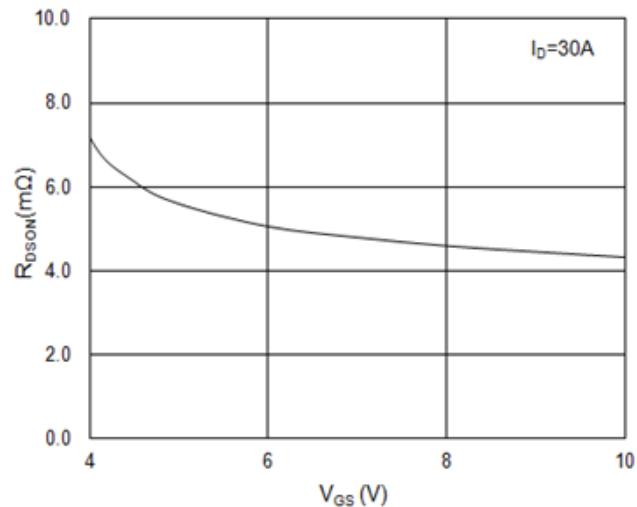


Fig.2: On-Resistance vs. Gate-Source

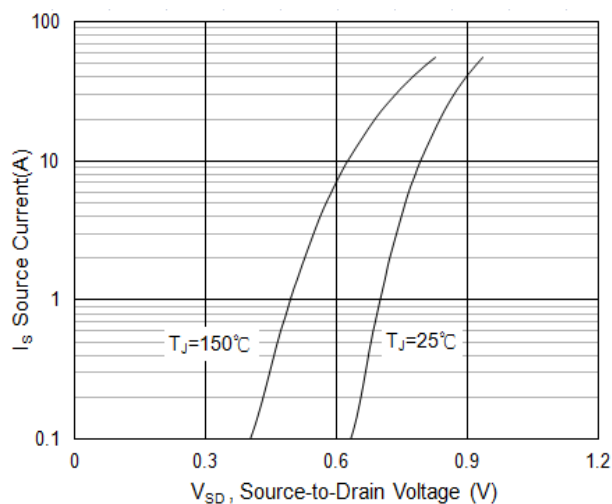


Fig.3: Forward Characteristics of Reverse

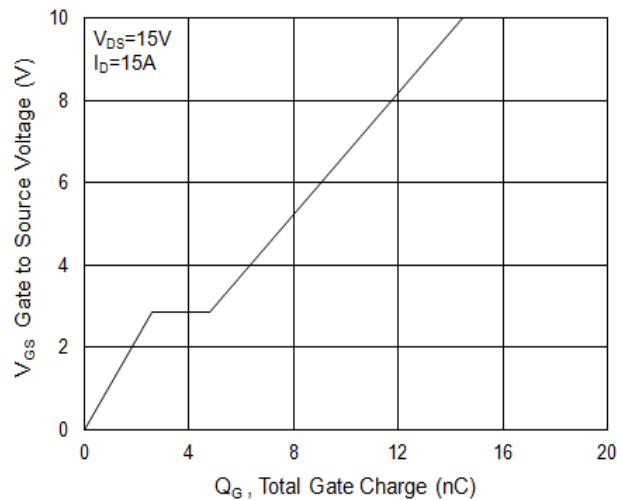


Fig.4: Gate-Charge Characteristics

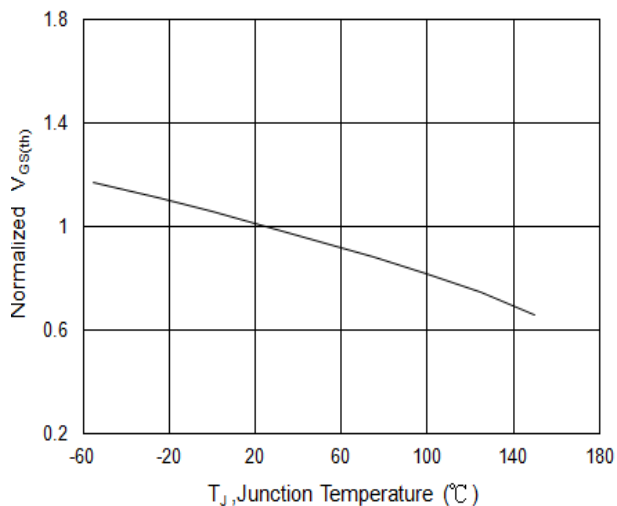


Fig.5: Normalized $V_{GS(th)}$ vs. T_J

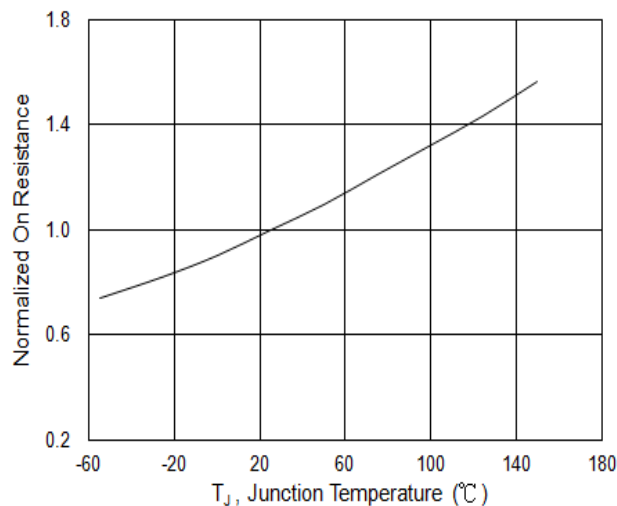


Fig.6: Normalized $R_{DS(on)}$ vs. T_J

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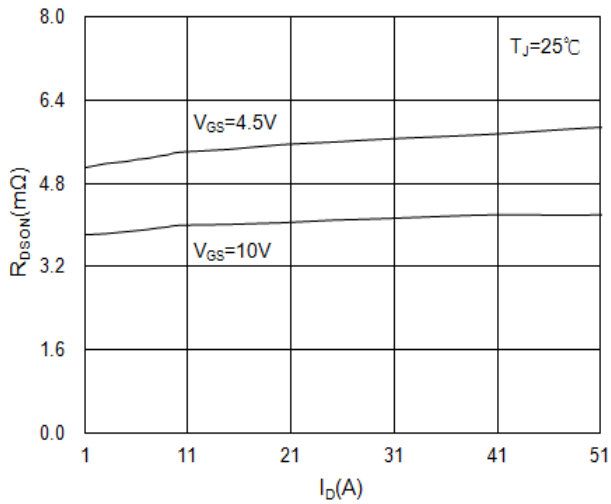


Fig.7: Drain-Source On-State Resistance

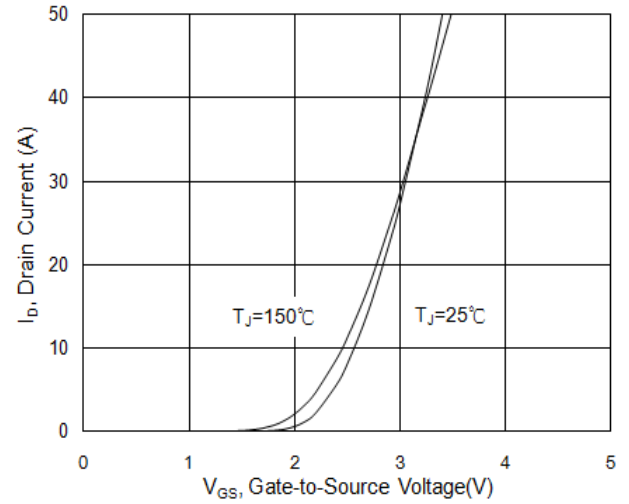


Fig.8: Transfer Characteristics

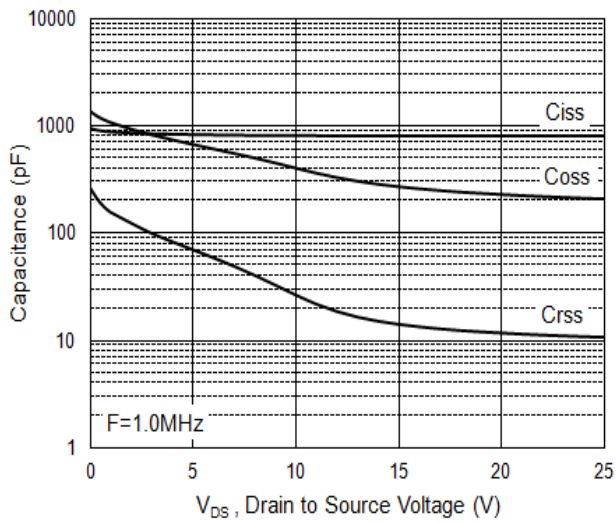


Fig.9: Capacitance

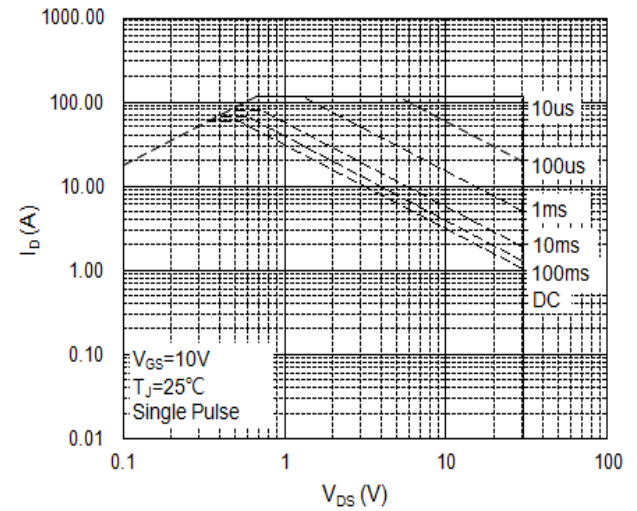


Fig.10: Safe Operating Area

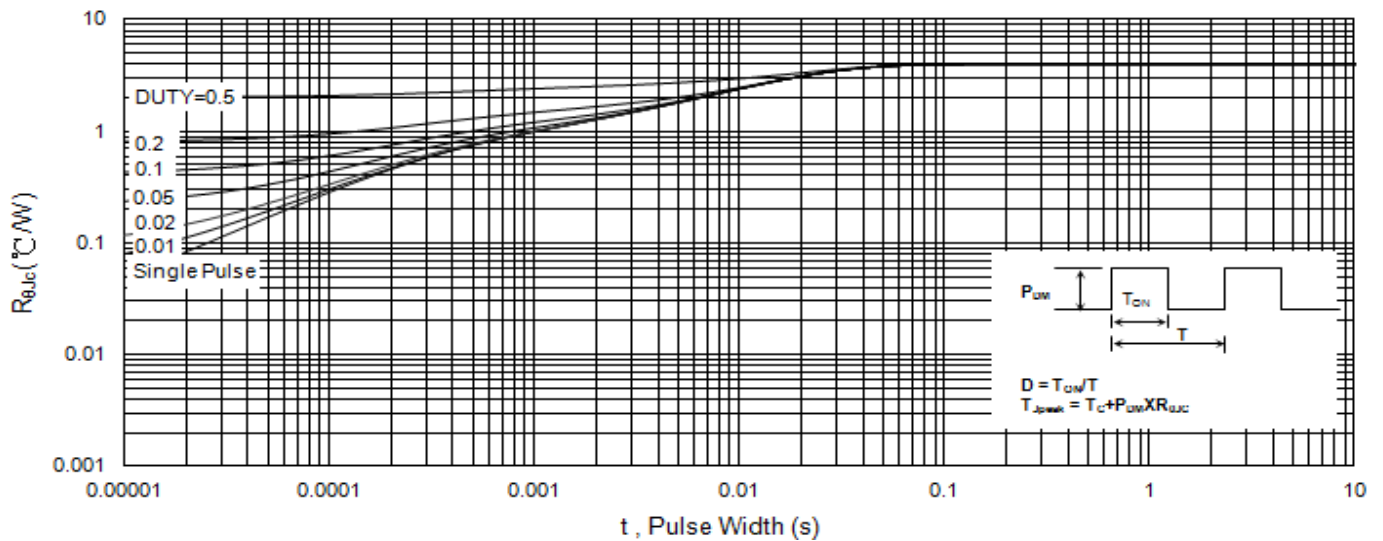
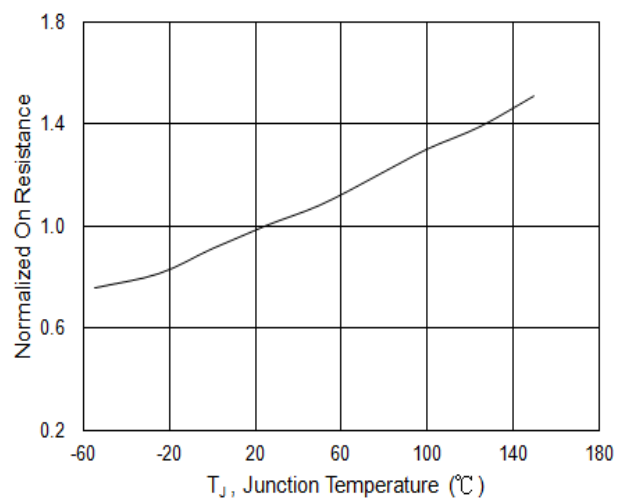
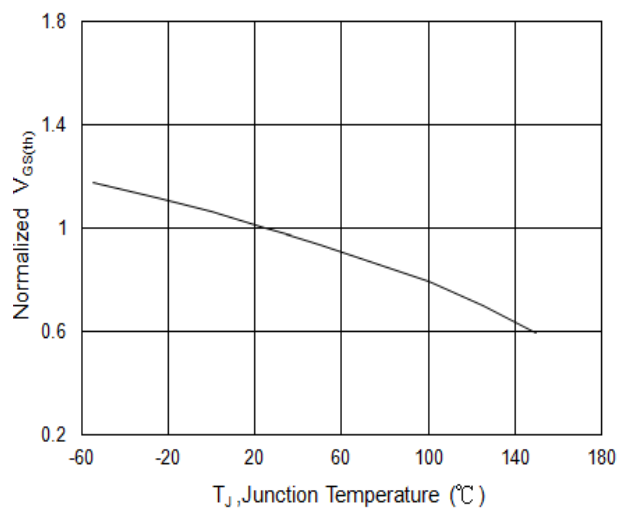
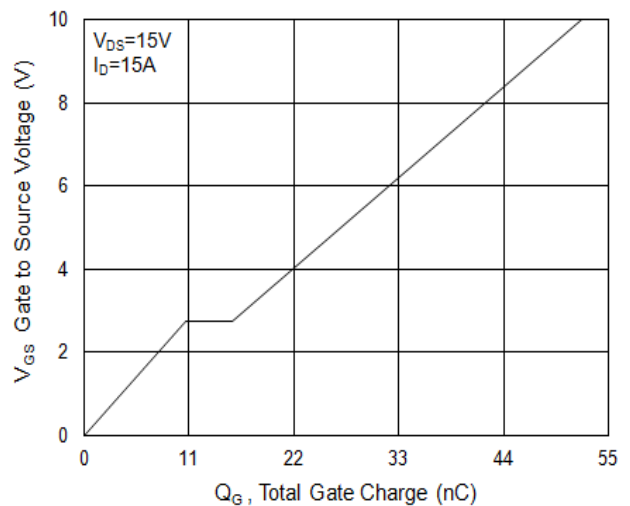
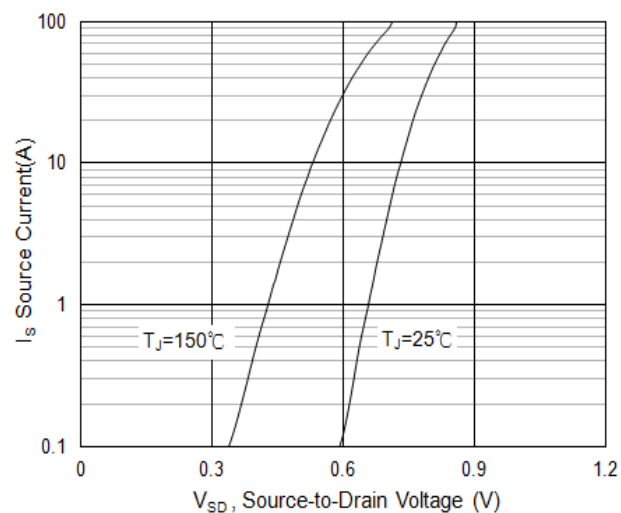
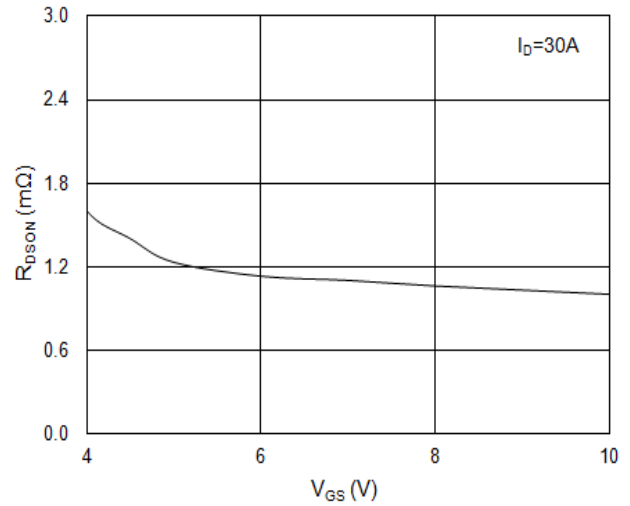
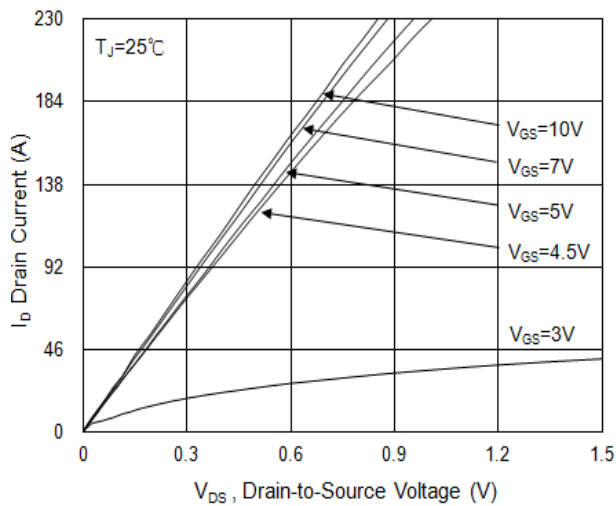


Fig.11: Transient Thermal Impedance

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Die2 Typical Characteristics



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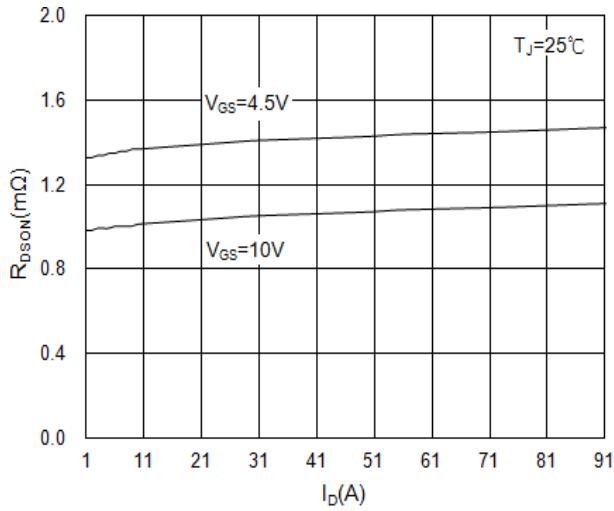


Fig.7: Drain-Source On-State Resistance

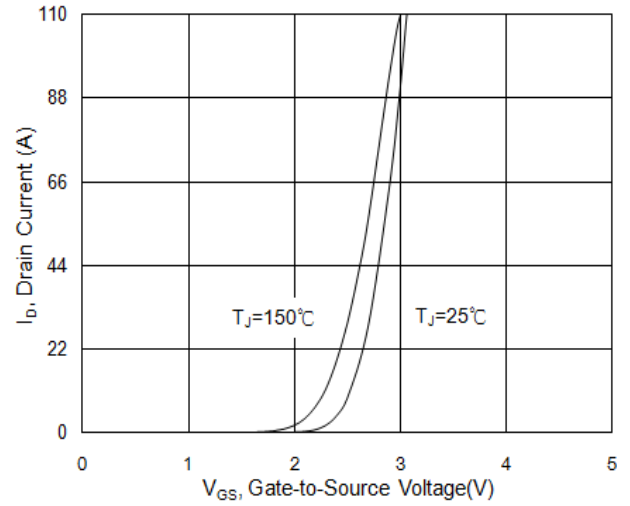


Fig.8: Transfer Characteristics

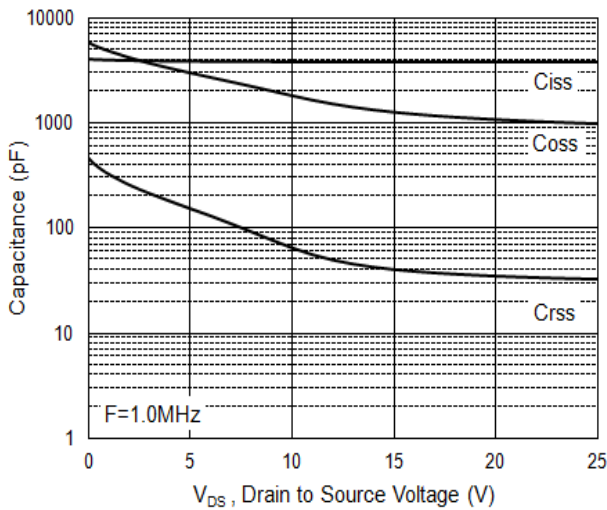


Fig.9: Capacitance

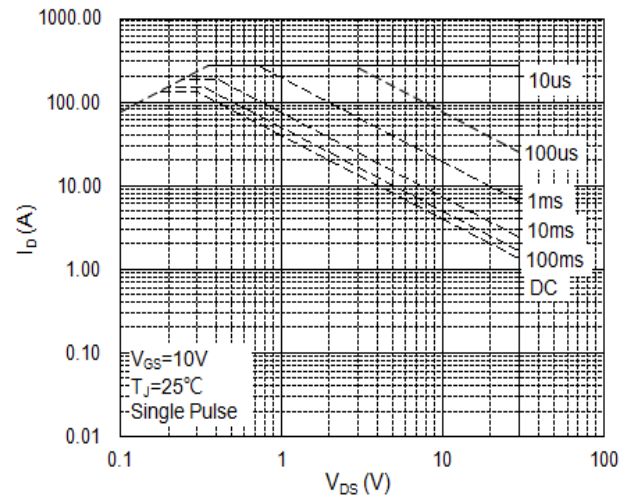


Fig.10: Safe Operating Area

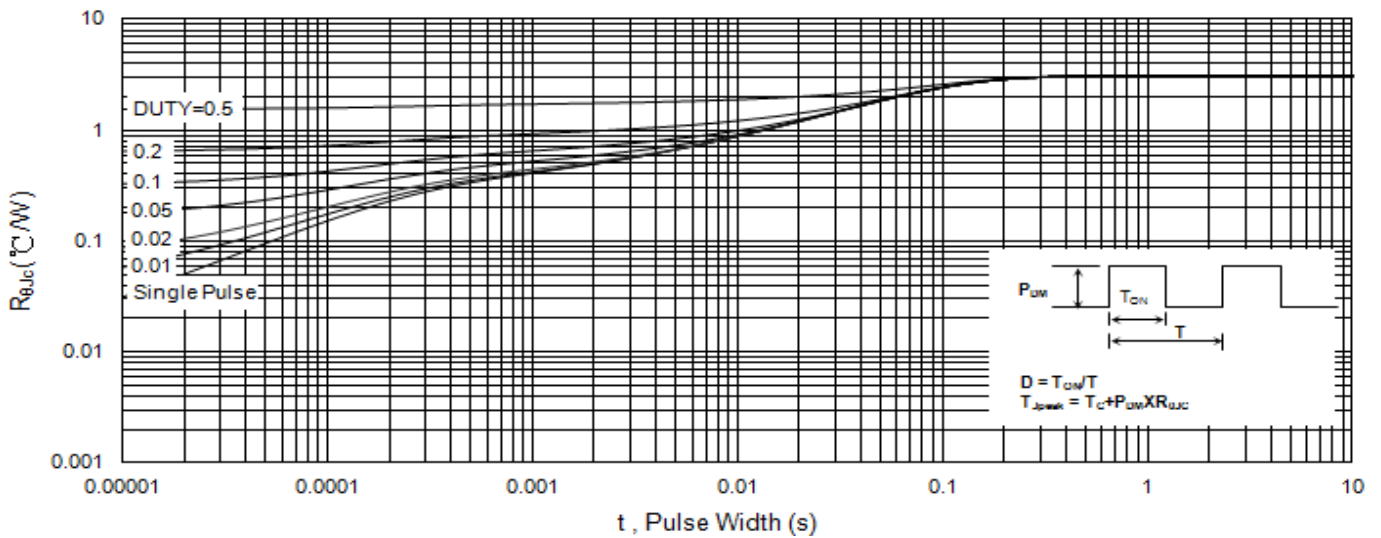


Fig.11: Transient Thermal Impedance

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