

Small Signal MOSFET

115 mA, 60 V

N-Channel SOT-323

- We declare that the material of product compliance with RoHS requirements.
- ESD Protected:1000V

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	60	V _{dc}
Drain-Gate Voltage ($R_{GS} = 1.0 \text{ M}\Omega$)	V_{DGR}	60	V _{dc}
Drain Current	I_D	± 115	mAdc
– Continuous $T_C = 25^\circ\text{C}$ (Note 1.)	I_D	± 75	
– Pulsed (Note 2.)	I_{DM}	± 800	
Gate-Source Voltage	V_{GS}	± 20	V _{dc}
– Continuous	V_{GSM}	± 40	V _{pk}
– Non-repetitive ($t_p \leq 50 \mu\text{s}$)			

THERMAL CHARACTERISTICS

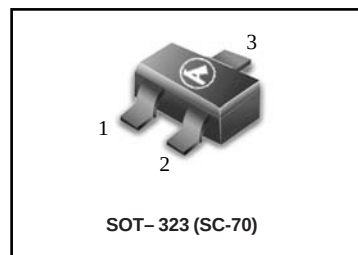
Characteristic	Symbol	Max	Unit
Total Device Dissipation FR-5 Board (Note 3.) $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	225 1.8	mW mW/ $^\circ\text{C}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	556	$^\circ\text{C/W}$
Total Device Dissipation Alumina Substrate, (Note 4.) $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	300 2.4	mW mW/ $^\circ\text{C}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	417	$^\circ\text{C/W}$
Junction and Storage Temperature	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$

1. The Power Dissipation of the package may result in a lower continuous drain current.
2. Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2.0\%$.
3. FR-5 = $1.0 \times 0.75 \times 0.062 \text{ in.}$
4. Alumina = $0.4 \times 0.3 \times 0.025 \text{ in}$ 99.5% alumina.

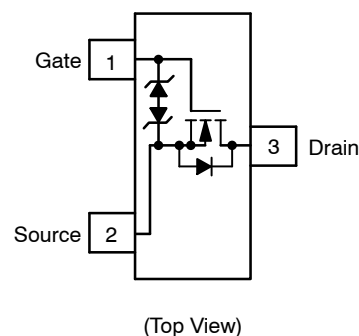
ORDERING INFORMATION

Device	Marking	Shipping
L2N7002WT1G	6C	
L2N7002WT3G	6C	10000 Tape & Reel

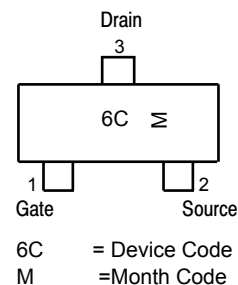
L2N7002WT1G



Simplified Schematic



MARKING DIAGRAM & PIN ASSIGNMENT



L2N7002WT1G
ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage ($V_{GS} = 0$, $I_D = 10\ \mu\text{Adc}$)	$V_{(BR)DSS}$	60	–	–	Vdc
Zero Gate Voltage Drain Current ($V_{GS} = 0$, $V_{DS} = 60\ \text{Vdc}$)	I_{DSS}	–	–	1.0	μAdc
		–	–	500	
Gate–Body Leakage Current, Forward ($V_{GS} = 20\ \text{Vdc}$)	I_{GSSF}	–	–	1	μAdc
Gate–Body Leakage Current, Reverse ($V_{GS} = -20\ \text{Vdc}$)	I_{GSSR}	–	–	-1	μAdc

ON CHARACTERISTICS (Note 2.)

Gate Threshold Voltage ($V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{Adc}$)	$V_{GS(th)}$	1.0	1.6	2.5	Vdc
On–State Drain Current ($V_{DS} \geq 2.0\ V_{DS(on)}$, $V_{GS} = 10\ \text{Vdc}$)	$I_{D(on)}$	500	–	–	mA
Static Drain–Source On–State Voltage ($V_{GS} = 10\ \text{Vdc}$, $I_D = 500\ \text{mAdc}$) ($V_{GS} = 5.0\ \text{Vdc}$, $I_D = 50\ \text{mAdc}$)	$V_{DS(on)}$	–	–	3.75	Vdc
		–	–	0.375	
Static Drain–Source On–State Resistance ($V_{GS} = 10\ \text{V}$, $I_D = 500\ \text{mAdc}$) $T_C = 25^\circ\text{C}$ $T_C = 125^\circ\text{C}$ ($V_{GS} = 5.0\ \text{Vdc}$, $I_D = 50\ \text{mAdc}$) $T_C = 25^\circ\text{C}$ $T_C = 125^\circ\text{C}$	$r_{DS(on)}$	–	1.4	7.5	Ohms
		–	–	13.5	
		–	1.8	7.5	
		–	–	13.5	
Forward Transconductance ($V_{DS} \geq 2.0\ V_{DS(on)}$, $I_D = 200\ \text{mAdc}$)	g_{FS}	80	–	–	mmhos

DYNAMIC CHARACTERISTICS

Input Capacitance ($V_{DS} = 25\ \text{Vdc}$, $V_{GS} = 0$, $f = 1.0\ \text{MHz}$)	C_{iss}	–	17	50	pF
Output Capacitance ($V_{DS} = 25\ \text{Vdc}$, $V_{GS} = 0$, $f = 1.0\ \text{MHz}$)	C_{oss}	–	10	25	pF
Reverse Transfer Capacitance ($V_{DS} = 25\ \text{Vdc}$, $V_{GS} = 0$, $f = 1.0\ \text{MHz}$)	C_{rss}	–	2.5	5.0	pF

SWITCHING CHARACTERISTICS (Note 2.)

Turn–On Delay Time	($V_{DD} = 25\ \text{Vdc}$, $I_D \cong 500\ \text{mAdc}$, $R_G = 25\ \Omega$, $R_L = 50\ \Omega$, $V_{gen} = 10\ \text{V}$)	$t_{d(on)}$	–	7	20	ns
Turn–Off Delay Time		$t_{d(off)}$	–	11	40	ns

BODY–DRAIN DIODE RATINGS

Diode Forward On–Voltage ($I_S = 115\ \text{mAdc}$, $V_{GS} = 0\ \text{V}$)	V_{SD}	–	–	-1.5	Vdc
Source Current Continuous (Body Diode)	I_S	–	–	-115	mAdc
Source Current Pulsed	I_{SM}	–	–	-800	mAdc

 2. Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$.

L2N7002WT1G

TYPICAL ELECTRICAL CHARACTERISTICS

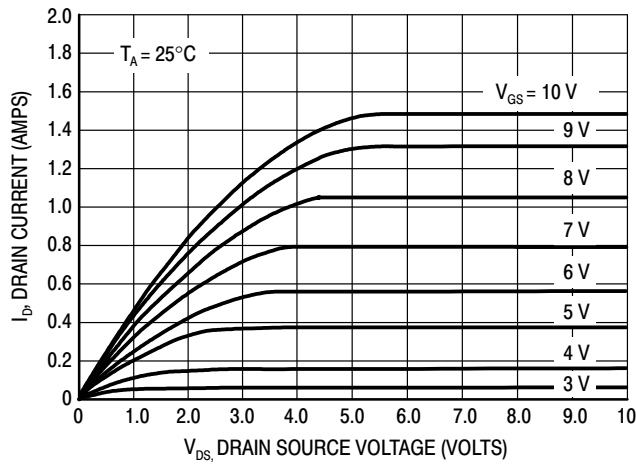


Figure 1. Ohmic Region

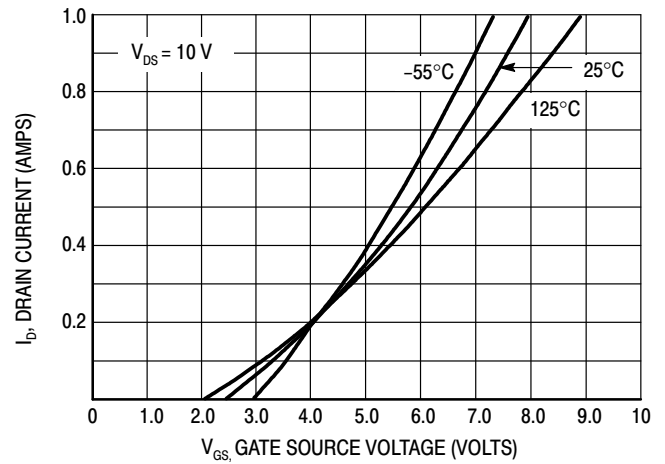


Figure 2. Transfer Characteristics

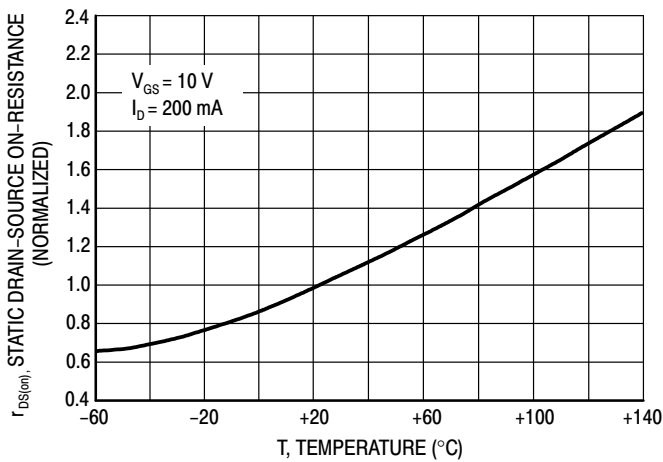


Figure 3. Temperature versus Static Drain-Source On-Resistance

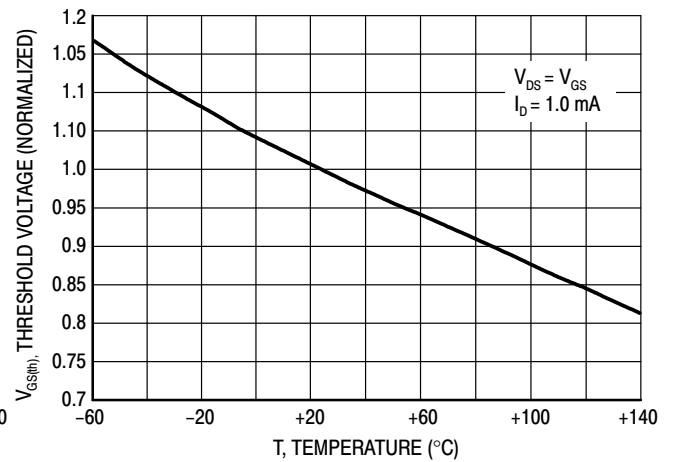
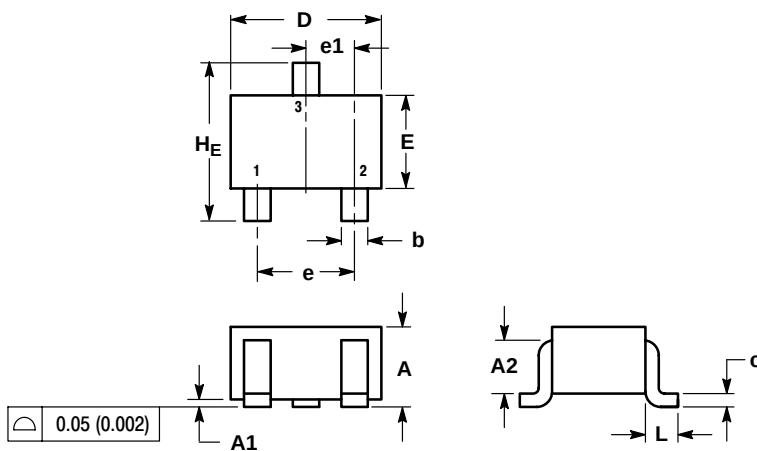
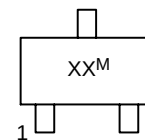


Figure 4. Temperature versus Gate Threshold Voltage

L2N7002WT1G
SC-70 (SOT-323)

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.90	1.00	0.032	0.035	0.040
A1	0.00	0.05	0.10	0.000	0.002	0.004
A2	0.7 REF			0.028 REF		
b	0.30	0.35	0.40	0.012	0.014	0.016
c	0.10	0.18	0.25	0.004	0.007	0.010
D	1.80	2.10	2.20	0.071	0.083	0.087
E	1.15	1.24	1.35	0.045	0.049	0.053
e	1.20	1.30	1.40	0.047	0.051	0.055
e1	0.65 BSC			0.026 BSC		
L	0.425 REF			0.017 REF		
H	2.00	2.10	2.40	0.079	0.083	0.095

GENERIC MARKING DIAGRAM


- XX = Specific Device Code
- M = Date Code
- = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

SOLDERING FOOTPRINT*
